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DH11 asynchronous 16-line multiplexer maintenance manual

digital

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DH11 asynchronous 16-line multiplexer maintenance manual

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INTRODUCTION

This manual provides the user with information concerning the installation, operation, and maintenance of the DH11 Asynchronous 16-Line Programmable Multiplexer.

Although signals are transferred between the DH11 and the PDP-11 Unibus, this manual does not provide detailed information on the operation of the Unibus. A detailed discussion of the Unibus is contained in the *PDP-11 Peripherals Handbook.*

Five chapters and four appendices comprise this manual:

Chapter 1	General Description
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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The DH11 Asynchronous 16-Line Programmable Multiplexer connects the PDP-11 with 16 asynchronous serial communications lines operating with individually programmable parameters. These parameters are:

Character Length: 5, 6, 7, or 8 bit

Number of Stop Bits: 1 or 2 for 6, 7, 8 bit characters
1 or 1.5 for 5 bit characters

Parity Generation and Detection: odd, even, or none

Operating Mode: half duplex or full duplex

Transmitter Speed and Receiver Speed: 0, 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800 or 9600 Baud plus Ext A, Ext B

Breaks: May be detected or generated on each line.

The DH11 multiplexer uses 16 double-buffered MOS/LSI receivers to assembly the incoming characters. An automatic scanner takes each received character and the line number and deposits that information in a first-in, first-out buffer memory referred to as the *silo*. The bottom of the silo is a register which is addressable from the Unibus.

The transmitter in the DH11 also uses double-buffered MOS/LSI units. They are loaded directly from message tables in the PDP-11 memory by means of single-cycle direct memory transfers (NPR). The current addresses and byte counts for each line's message table are stored in semiconductor memories located in the DH11. This reduces the Unibus time taken for the NPR transfers to one NPR cycle per character transmitted. The NPR cycle used is lengthened slightly.

As many as 16 DH11s may be placed on a single PDP-11 processor, creating a total capacity of 256 lines. Figure 1-1 shows some typical DH11 system applications.

1.1.1 DH11-AA and -AC Line Interfaces

Four DM11-DAs are connected to a DH11-AA or AC. Each DM11-DA provides line conditioning for four serial communications devices using 20 mA current loops. Such devices include a Teletype®, LA36 or VT05A or B.

Four DM11-DBs are connected to a DH11-AA or AC. Each DM11-DB provides line conditioning for four EIA/CCITT devices not requiring modem control.

® Teletype is a registered trademark of Teletype Corporation.

Four DM11-DCs are connected to a DM11-BB Modem Control which in turn is connected to a DH11-AA or AC. Each DM11-DC provides line conditioning for four EIA/CCITT devices equipped with data set control.

1.1.2 DH11-AB Line Interfaces

A DC08 Telegraph Line Interface is used with two DH11-ABs to provide line conditioning for 32 telegraph lines.

1.1.3 DH11-AD and -AE Line Interfaces

The DH11-AD and -AE use the H317-B distribution panel which provides 16 EIA/CCITT lines for devices with or without data set control.

1.2 PHYSICAL DESCRIPTION

1.2.1 Configurations

The DH11-AA multiplexer is available in four variations as shown in Figure 1-2:

The DH11-AA consists of a double system unit, all modules necessary to implement a 16-line asynchronous multiplexer, a 5-1/4 inch level conversion and distribution panel with its own power supply, and a data cable between the logic in the double system unit and the level conversion/distribution panel. The modules for level conversion are not included, so that the type and quantity of lines may be customized to the customer's requirements. The power supply for the distribution panel is also 5-1/4 inches high. Generally, it can be mounted on the rear of the rack in a position opposite the distribution panel, which is usually mounted on the front of the rack.

The DH11-AB is the same as the DH11-AA, but does not include the level conversion/distribution panel or its associated power supply. Instead of a data cable to a distribution panel, a data cable to the DC08CS Telegraph Converter Panel is supplied.

The DH11-AC is the same as the DH11-AA, except that the power supply on the level conversion/distribution panel is arranged for 240 V, 50 Hz operation. (There is no need for a 50 Hz version of the DH11-AB because it is a processor-powered option).

All of the above versions of the DH11 include pre-wired slots in the double system unit for the insertion of a DM11-BB Modem Control option.

The DH11-AD consists of a double system unit, all modules necessary to implement a 16-line asynchronous multiplexer, EIA level conversion for the data lines, modem control with EIA conversion, and a 16-line EIA distribution panel.

The DH11-AE is the same as the DH11-AD except the modem control is not included.

CAUTION

The DH11 uses hex modules and thus cannot be mounted in a BA11 CS or ES Expander Box. The 11/35, 11/40, 11/45 type boxes must be used (BA11-B, D, F series).

1.2.2 Multiplexer Distribution Panel and Power Supply

The DH11-AA and AC provide a panel for level converters and cables for the individual lines. The panel uses a standard H911 style rack, but only 6 connector blocks are used.

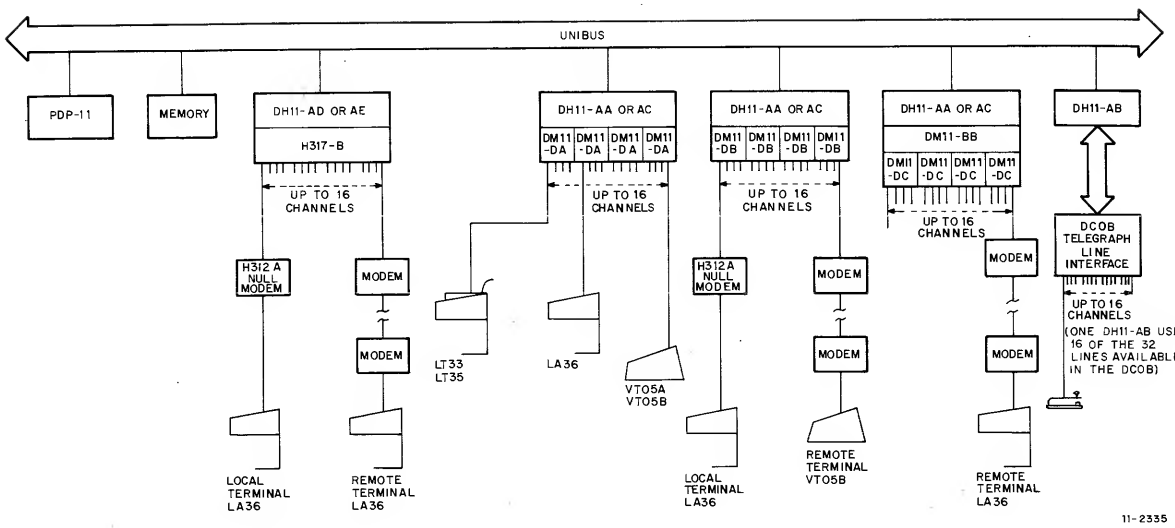


Figure 1-1 DH11 System Applications

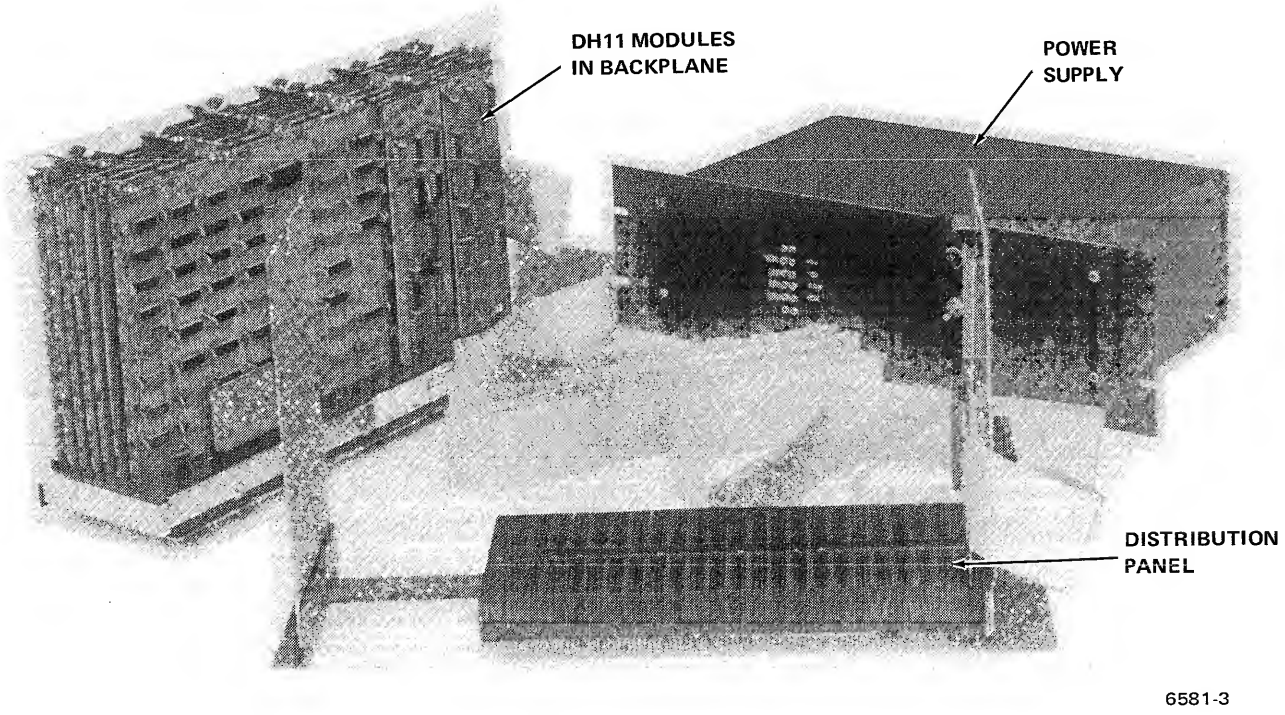
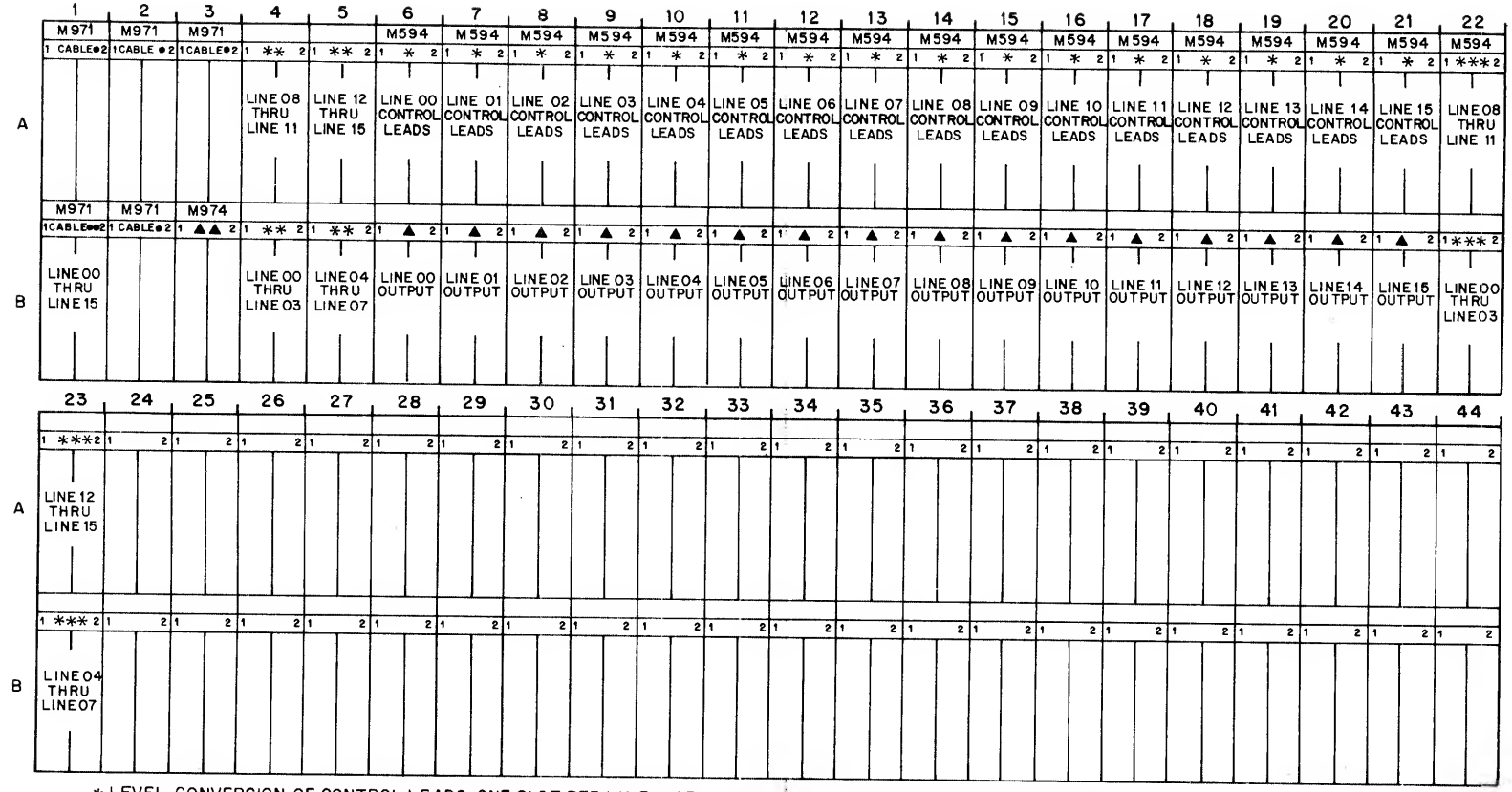


Figure 1-2 DH11 Multiplexer



* LEVEL CONVERSION OF CONTROL LEADS. ONE SLOT PER LINE. USE M594 ONLY WHEN DM11-BB IS IMPLEMENTED. IF DM11-DB IS USED REPLACE M594 WITH W404-A (SUPPLIED WITH DM11-DB). IF DM11-DA IS USED LEAVE BLANK.

** USE M594 FOR DM11-DB

*** USE M596 FOR DM11-DA

● USE ONLY IF DM11-BB IS IMPLEMENTED

●● DATA CABLE FROM DH11-AA CONTROL LOGIC

▲16 CABLE SLOTS ONE PER LINE FOR DM11-DA USE M973, FOR DM11-DB USE BC01R-25

▲▲ JUMPER CARD USED FOR DIAGNOSTIC PROGRAMS ONLY, REMOVE FOR NORMAL OPERATION

11-2206

Figure 1-3 Distribution Panel Module Utilization Diagram

The slot assignments follow the DF11 format which is the standard level conversion and cable slot for PDP-11 Communications Products (Figure 1-3). Slots A06 through A21 are used for level conversion modules. Slots B06 through B21 are used for cable termination. Other slots provide inputs or special purpose outputs. The distribution panel mounts on a standard 19-inch cabinet and connects to the DH11 logic by means of a BC08-S Data Cable.

Power for the distribution panel is provided by the H758 Power Supply mounted on the rear of the cabinet. Some units in the field use H739 or H751 supplies which are generally equivalent to an H758 supply. The H758 provides the voltages listed below:

+15 V @ 2 A
-15 V @ 2 A
+5 V @ 4 A

Power drain of the distribution panel depends on the type of level conversion used. The maximum drain on the +15 V and -15 V occurs when DF11-BB modems are used, at which time the full rated output of a 2 A is used. The maximum +5 V drain occurs when all lines are arranged for full modem control (four DM11-DC options); the current used is then 1.7 A.

The level conversion types can be mixed on a 4-line basis by using different converters on slots A4, A5, B4, and B5. Also, level converters can be mixed on a single line basis by using slots A6 through A21 for level conversion on a single line basis. Consult Figure 1-3 for specific details.

The DH11-AD and AE options use a 16-line EIA distribution panel. This panel requires no power of its own. It mounts in a standard 19 inch cabinet and connects to the DH11-AD and AE logic by means of two BC08S data cables and four BC08R modem control cables.

BC05D-25 cables may be ordered separately to connect from the EIA distribution panel to the modem.

1.2.3 General Specifications

Environmental:
Temperature: +50° F to +110° F
Humidity: 0 to 95 percent non condensing

Power Consumption:
The power consumption of the DH11-AA, AB, and AC logic (excluding the level conversion modules, which run off the level conversion/distribution panel power supply) is:

+5 V:	8.4 A (DH11 alone)**
	11.2 A (DH11 plus DM11-BB Modem Control)**
-15 V:	240 mA

The power consumption of the DH11-AD and AE is:

DH11-AD

+5 V:	10.8 A**
+15 V:	400 mA
-15 V:	645 mA

**Add 0.2 A if this is the last option on the Unibus.
(The Unibus terminator consumes 0.2 A)

DH11-AE

+5 V:	8.6 A**
+15 V:	100 mA
-15 V:	340 mA

**Add 0.2 A if this is the last option on the Unibus.
(The Unibus terminator consumes 0.2 A)

Receivers:

The DH11 receiver units provide serial to parallel conversion of 5, 6, 7, or 8 bit code with one start bit and at least one stop bit. An extra data bit is added when parity operation is selected. The allowable input distortion is 43.75 percent assuming no speed distortion. The maximum allowable speed distortion is 4.8 percent for 8-bit characters.

The DH11 transmitter units provide parallel to serial conversion of 5, 6, 7, or 8 bit code with one start bit and one, one and a half (5 bit only), or two (6, 7, or 8 bit only) stop units. An extra data bit is added if parity operation is selected.

The number of bits per character, the number of stop marks, and parity mode are selectable on a per-line basis, but must be the same as the corresponding receiver. The serial data rate is determined by a crystal clock and is program controllable on a per-line basis. The transmitter speeds may be program controlled independently of the receiver speeds. Output distortion is less than 2 percent.

Interface:

Interface to and from the control section. There are 16 output data lines and 16 input data lines at TTL levels using negative logic (mark = 0).

The input leads from the level conversion/distribution panel are equipped with pull up resistors which place lines not equipped with level conversion in a permanently spacing condition. Logic in the DH11 receivers prevents this condition from assembling null characters on a continuous basis, however.

Bus Loading:

The DH11 presents two bus loads to the Unibus. If a Modem Control is added, an additional bus load is added.

1.3 FUNCTIONAL DESCRIPTION

1.3.1 Receiver Operation

Reception on each line is by means of Universal Asynchronous Receiver/Transmitters (UARTs). These are 40-pin MOS/LSI devices that perform all the necessary functions for double-buffered asynchronous character assembly.

The receiver section of the UART samples the line at 16 times the bit rate of the signals to be received on that line. Upon detection of a mark-to-space transition, the UART counts 8 clock pulses and checks the state of the line again. This sampling occurs in the center of a normal start bit. If that sample is a mark, the receiver returns to its idling state, ready to detect another mark-to-space transition. If the sample is a space, the receiver enters the data entry condition and samples the state of the line at subsequent sample points spaced at multiples of 16 clock ticks from the center of the start bit. The number of samples taken is determined by the character length information entered into the UART via the Line Parameter Register. If parity checking has been enabled for this line, the receiver computes the parity of the character just received and compares it with the parity sense specified for reception on that line. If the parity sense differs, the parity error bit is set.

The character length, parity sense, number of stop bits, etc., that are used by the UART to perform the above operations, are stored within each UART in a Control Bits Holding Register. The Control Bits Holding Registers of each UART are addressable, on a write-only basis, from the Unibus, by first setting the line selection bits of the System Control Register and then loading the desired line parameters into the Line Parameter Register, from which they are automatically transferred to the Control Bits Holding Register of the designated UART. It is important that no interrupt handling routine intervene and change the contents of the System Control Register during the above operation.

1.3.2 Silo Operation

The silo is an MOS/LSI digital storage buffer that is 16 bits wide and 64 words deep. A 16-bit word is entered at the top and automatically bubbles down to the lowest location that does not already contain an entry. The bottom of the silo is the Next Received Character Register (NRC).

There are three registers associated with the silo. One is the Next Received Character Register. It is a read-once register because it is the bottom of the silo, and reading it extracts that character from the silo and causes all other entries to bubble down one more position.

The other two registers are byte-size registers and are contained within the Silo Status Register. One is the high byte, which is read-only and contains the status of an up-down counter, giving the actual fill level of the silo. The second register, the low byte, is read/write and is used by the program to specify that silo fill level beyond which the program wishes to receive interrupt notification.

1.3.3 Transmitter Operation

In the transmit mode, the program picks the desired line and selects the transmitter operating parameters. The program then loads the Current Address Register (CAR) with the memory address of the first character to be transmitted on the selected line. It also loads the Byte Count Register (BC) with the number of characters in the message and sets the bit of the Buffer Active Register (BAR) associated with the selected line. When the transmitter scanner finds a Transmitter Buffer Empty (TBMT) flag high for the selected line, it stops and a character is transferred from memory to the UART for transmission.

Transmission on each line is by means of UARTs that perform all the necessary functions for double-buffered asynchronous character transmission. The transmitter section of the UART holds the serial output line at a marking state when idle. When the transmitter loading leads have been conditioned with the character to be transmitted and the data strobe lead has been brought high (these functions are performed by the NPR control), the UART commences generation of a start space within one sixteenth of a bit time. The start space and all subsequent data bits are a full bit time each. The start space is followed by M data bits, where M is 5, 6, 7, or 8, as determined by the

Control Bits Holding Register. The data bits are presented to the line least significant bit first. The parity bit, if parity generation is enabled, is calculated by the transmitter and affixed after the last data bit, but before the stop marks.

The stop bit or bits depend in quantity upon the setting of the control word. If the transmission of 6, 7, or 8 bits has been selected, the program may select either one or two stop bits. If the transmission of 5 bit code has been selected, the program may select either one or one and a half stop bits.

If the transmitter's holding register has been loaded while a character was being transmitted, the second character has its start bit commence immediately at the end of the preceding character's stop bit(s).

1.3.4 Auto-Echo Operation

The DH11 contains provision for the hardware to echo received characters without software intervention. The feature may be enabled on any line by conditioning the line selection bits in the System Control Register and then setting the appropriate bits in the Line Parameter Register, including bit 15 (Auto Echo Enable).

The auto-echo hardware is part of the receiver scanner and operates as follows:

a. If the receiver scanner finds a received character for a line upon which auto-echo is not enabled, it simply dumps that character into the silo and resumes scanning.

b. If the receiver scanner finds a received character for a line upon which auto-echo is enabled, it examines the error flags associated with that character.

    1. If a framing error is detected, the remote terminal is trying to gain the attention of the processor by sending a break. In this case, the auto-echo hardware dumps the received character and associated flag into the silo so that the system software is alerted. The break is not echoed to the remote terminal.

    2. If an overrun error is detected, the remote terminal is trying to gain the attention of the processor by typing characters. This case is treated identically to b1, above.

c. If the receiver scanner finds a received character from a line upon which auto-echo is enabled and there are no error flags of the type mentioned above, the receiver scanner and auto-echo logic attempts to echo the character. First, however, certain tests of internal logic conditions must be made.

    1. The UART transmitters are all loaded from a common internal data bus. Therefore, the auto-echo hardware must first check to see that no NPR cycles are in progress, loading a UART transmitter from that bus. If a conflict is indicated, the receiver scanner is restarted and the process is tried again on the scanner's next rotation.

    2. If the above test indicates no problem, the one remaining check is to see if the Transmitter Holding Register for the line upon which the character was received is available. If it is not, the scanner is restarted. If it is available, auto-echo commences.

    It is not advisable to transmit messages on a line and auto-echo characters received on that line simultaneously. It is not possible to receive characters on a line at 30 characters per second, echo them back by auto-echo at 30 characters per second, and transmit an independent message at 30 characters per second, all on the same line. The auto-echo hardware will interlock these functions to some degree, but if more than two characters are received on a line while the scanner is waiting for the transmitter holding buffer to become available, a data overrun occurs and characters are lost. Auto-echo and software-driven transmission should not be attempted on the same line simultaneously, if input from that line is expected.

1.3.5 Interrupts

1.3.5.1 Receiver Interrupts – There are two kinds of receiver interrupts; they are enabled by bits 6 and 12 of the System Control Register.

Receiver Interrupt (System Control Register bit 7) – This interrupt, when enabled, occurs whenever the number of entries in the silo exceeds the silo status alarm level that the program has stored in the low byte of the Silo Status Register and SCR bit 6 is set. (The program can examine actual silo fill at any time by examining the high byte of the Silo Status Register.)

Storage Overflow Interrupt (System Control Register bit 14) – This interrupt, when enabled, occurs when the character storage silo is full and the DH11 hardware needs to store an additional character and SCR bit 12 is set. Should this situation occur, it does not necessarily mean that data has been lost.

1.3.5.2 Transmitter Interrupts – There are two kinds of transmitter interrupt; both are enabled by bit 13 of the System Control Register.

Transmitter Interrupt (System Control Register bit 15) – This interrupt, if enabled, occurs whenever one or more lines have finished the transmission of a complete string of characters. Specifically, it occurs after the NPR cycle that loaded the last character to be transmitted (and hence incremented the byte count to 0).

Non-Existent Memory Interrupts (System Control Register bit 10) – This interrupt, when enabled, occurs whenever the DH11 addresses non-existent memory. Specifically, this interrupt occurs if the DH11 enters an NPR cycle, places an address on the Unibus, and fails to receive a slave sync response for the location addressed within 20 μs.

CHAPTER 2
INSTALLATION

This chapter provides information for installing and testing a DH11. The information is given in procedural steps.

1. After unpacking, check that all parts are present for the particular configuration listed below.

List A

1	7009180 Wired Backplane Assembly
1	7009561 Power Harness
1	G727 Grant Continuity Card
2	BR 5 Jumpers (5408778)
2	M7821 Interrupt Control Modules
1	M796 Unibus Master Control Module
1	M4540 Crystal Clock Module
1	M7277 Current Address and Address Selection Module
1	M7278 Registers and Byte Control Module
1	M7279 FIFO Buffer Module
2	M7280 Multiple UART Cards
1	M7288 Line Parameter Control Module
1	M7289 System Control and Receiver Scanner Module

List B

2	M971 Cable Card (type BC08R)
1	BC08S Cable
1	7008456 Distribution Panel (7008443 Logic with End Panels)
1	7008493 Power Harness
1	H758A or H739A Power Supply

List C

2	BC08S Cables
2	H8611 Test Connectors
1	H315 Test Connector
1	M5906 Priority and EIA Conversion Module
1	H317B EIA Distribution Panel (5410260 EIA Distribution Panel, 7410667-2 Cover, two 7410668 Cable Clamps, and a 7410666 Mounting Plate)

DH11-AA: The items in lists A and B, one G7360 Priority Selector Card, and one M974 Maintenance Board.

DH11-AB: The items in list A, one G7360 Priority Selector Card, one M974 Maintenance Board, and a 7008423 (M972 to dual W077) Cable.

DH11-AC: The items listed for the DH11-AA, but with an H758B or H739B (220 V) Power Supply substituted for the H758A or H739A Power Supply shown in list B. The DH11-AC is the 220 V version of the DH11-AA.

DH11-AD: The items in lists A and C, one M7807 Mux and Bus Control Module, one M7808 Mux and Scan Control Module, and a H861 Test Connector (Modem Control).

DH11-AE: The items in lists A and C.

2. In addition to the material mentioned above, the following items should be included.

   For each DM11DA ordered:

   1 M596 TTL to 20 mA Level Converter
   4 M973 Mate-N-Lok Cards

   For each DM11DB ordered:

   1 M594 TTL to EIA Level Converter
   4 BC01R Cable Assembly
   4 W404 DTR Jumper Card

   For each DM11DC ordered:

   4 M594 TTL to EIA Level Converter
   4 BC01R Cable Assembly

3. Refer to the unit assembly drawing (D-UA-DH11-0-0) in the DH11 Print Set. Install the DH11 9-slot double system unit containing the wired logic in a convenient spot in the expander box or processor box. With all power off, install the 7009561 Power Harness, being very careful to install the Faston connectors on their respective tabs without catching against or cutting any of the nearby backplane wiring. In early units, the long axis of the tabs is in line with the long axis of the double system unit. In this case, the power tabs must be bent so that they clear both the pins of the wired logic and the power supply regulators. The proper connections are listed on the backplane etch and their relative positions are shown in Figure 2-1. The DH11 interconnection diagrams are shown in Figures 2-2 and 2-3. When using the backplane with tabs whose long axis is perpendicular to the long axis of the system unit, the 7009561 Power Harness is used without alteration.

   Secure the ground wire from F02T1 to one of the mounting screws. Do not plug in the white connector of the 7009561 until step 9.

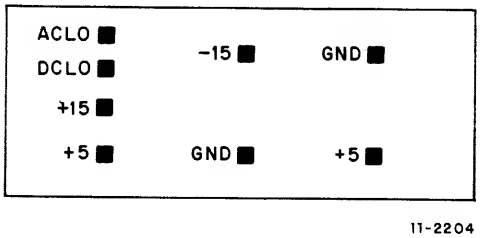


Figure 2-1 Backplane to 7009561 Cable Interconnection

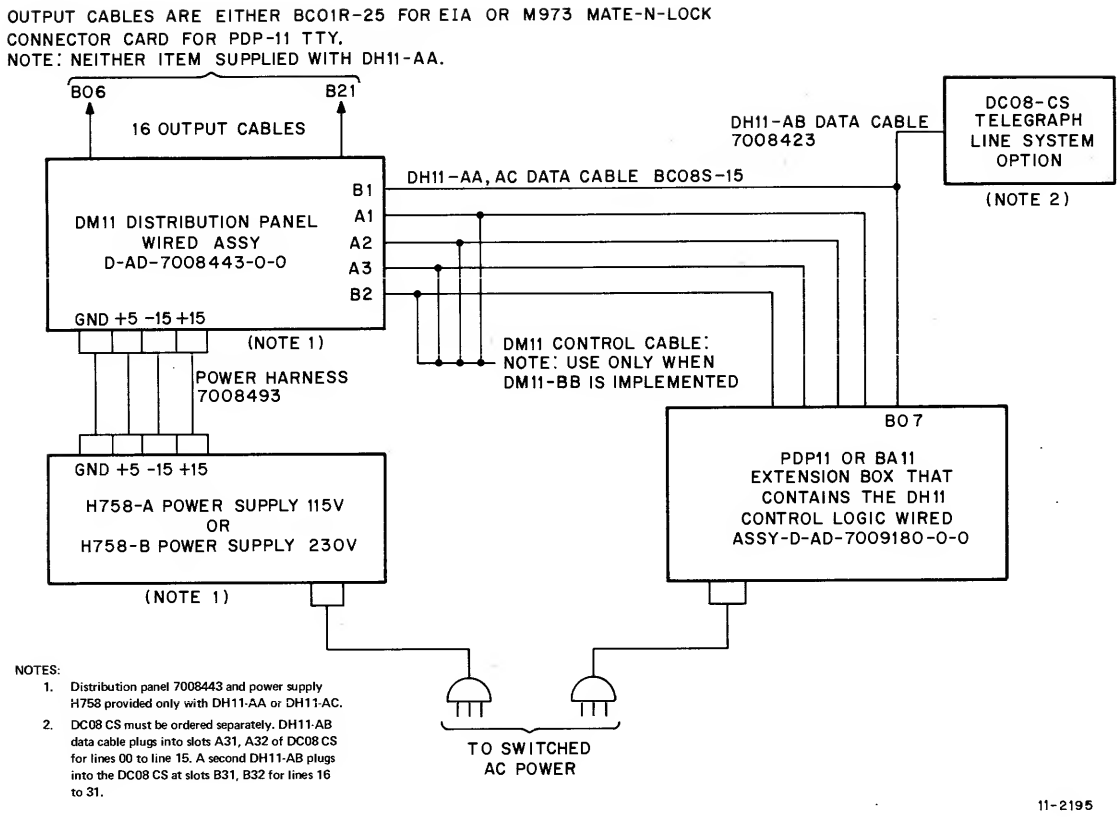


Figure 2-2 DH11-AA, AB, and AC Interconnection Diagram

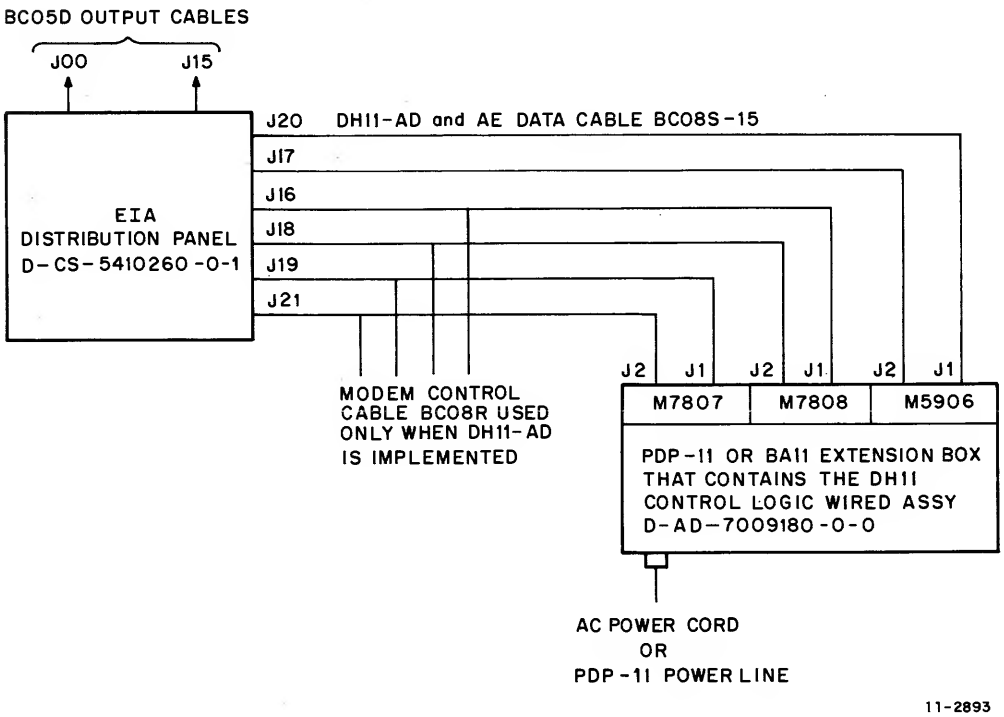


Figure 2-3 DH11-AD and AE Interconnection Diagram

4. Install the modules in their proper locations according to the module utilization list (D-MU-DH11-3-0). Figure 2-4 is the module utilization diagram. It is helpful to place the Unibus connectors, Unibus terminator (if used as last unit), and any modules with cables attached first. Beware of the tendency of hex modules to bow in the middle and for hex module extractor handles to catch on adjacent conventional handles.

5. Be sure that the G7360 or M5906 card has both priority plugs in place. BR5 is standard for the DH11.

6. The DH11 uses floating addresses and is located after the DJ11s in the floating address space that begins at location 160010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11s in a system should have consecutive addresses.

   Example 1: A system with no DJ11s, but two DH11s:

   160010 Cannot use for DH11s because not multiple of 20
   160020 First DH11
   160040 Second DH11
   160060 DH11 Gap (indicates that there are no more DH11s).

   Example 2: A system with one DJ11, two DH11s:

   160010 First DJ11
   160020 DJ11 Gap (indicates that there are no more DJ11s).
   160030 Cannot use for DH11s because not a multiple of 20.
   160040 First DH11
   160060 Second DH11
   160100 DH11 Gap (indicates that there are no more DH11s).

   The DH11 vectors (2) follow those of the DJ11 in the floating vector space that starts at address 300. The vectors starting at 300 are used in the following order: DC11; KL11/DL11-A,B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C,D,E; DJ11; DH11.

   Of the two vectors, the receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP-11 priority jumper plugs. If both are the same, the receiver has interrupt priority because it is electrically closer to the processor.

   If one or more DM11-BB options are ordered with the DH11s in a system, the DM11-BBs and associated DM11-DCs should be installed in the DH11s that have the lowest addresses (i.e., DH11-AA and ACs).

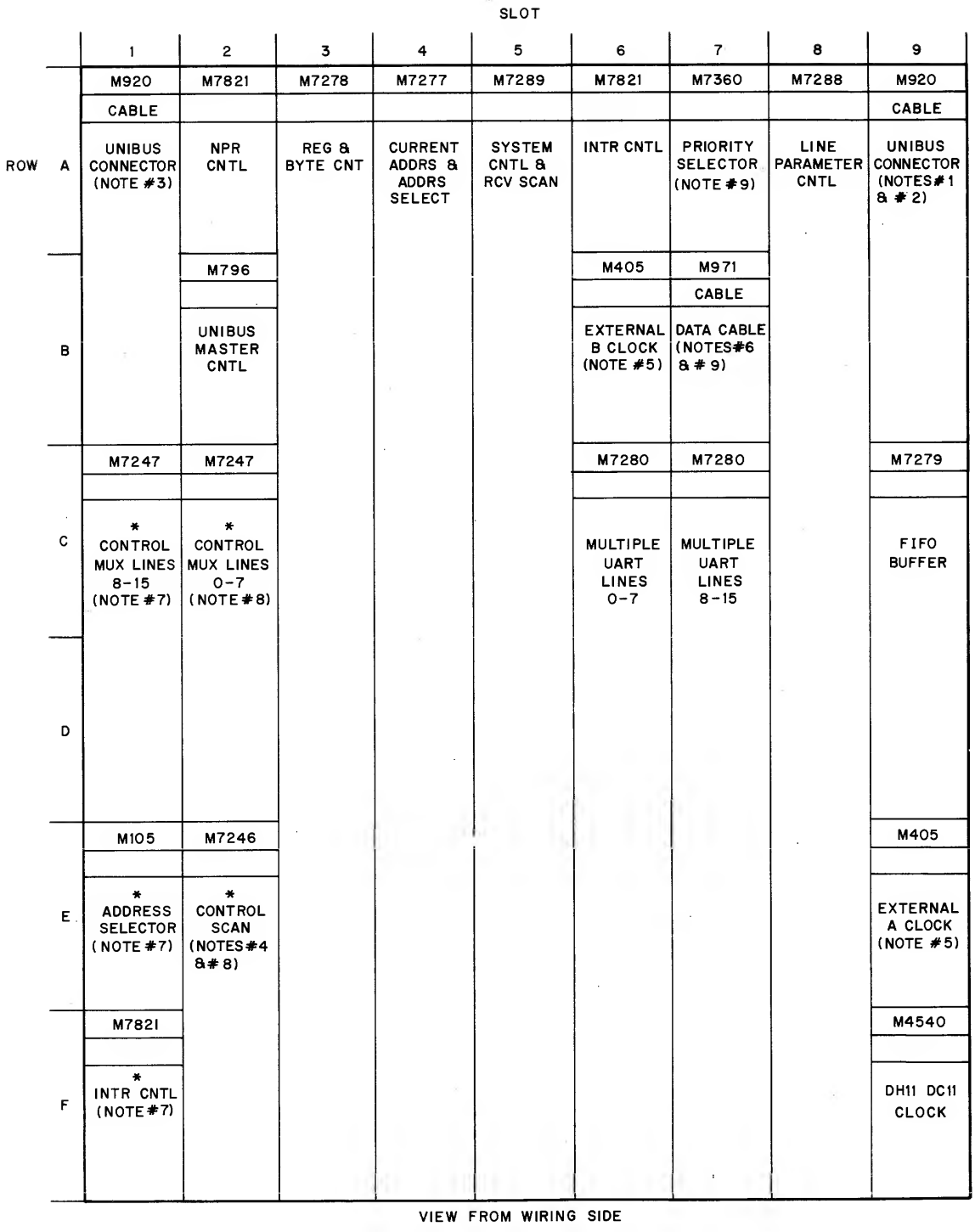
   The DH11s should be in order of increasing address as follows:

   1. DH11s with DM11-BB and full complement of DM11-DCs

   2. DH11-ADs

   3. DH11s with DM11-BB and a partial complement of DM11-DCs

   4. DH11s without modem control, but EIA conversion for data lines only (DM11-BBs or DH11-AEs)



NOTES:

1. If end of bus, replace M920 with M930.
2. If last unit in basic box, replace M920 with BC11A cable when expanding to peripheral box.
3. If first unit in expander box, replace M920 with BC11A cable.
4. E02 must be G727 grant continuity if modem control module set is not installed. * denotes DM11-BB modem control option, with DH11-AA or AC.
5. Module slots provide for additional clock rates.
6. For diagnostic checkout of DH11-AA, AB, or AC, replaces M971 with M974.
7. This slot contains Modem Control Module M7807 with DH11-AD.
8. This slot contains Modem Control Module M7808 with DH11-AD.
9. This slot contains EIA Converter and Priority Module M5906 for DH11-AD or AE.

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Figure 2-4 DH11 Module Utilization Diagram

5. DH11s with EIA and 20 mA mixed

6. DH11s with 20 mA only

The above order is preferred for RSTS systems. If the customer has other desires, he is the final authority.

7. The DH11 requires two M7821 modules. One of these modules (A06) is used to generate interrupts and must have its vector bit jumpers cut to provide the selected vector address.

Both sections of the M7821 are set to the same priority level (BR5) and each one generates an interrupt. Section A is used for receiver interrupts which assert the vector addresses of the form XX0, Section B is used for transmitter interrupts which assert vector addresses of the form XX4. To accomplish this, the bit 2 jumper must be left in. (If a DM11-BB is installed, its M7821 module (slot F01) must have the bit 2 jumper cut.) The other jumpers (bits 3–8) are cut as shown below to select the desired vector address. The jumper for vector bit 2 (W2) on the M7807 module must be out.

Jumper						Vector Address
8	7	6	5	4	3	
X			X	X	X	300
X			X	X		310
X			X		X	320
X			X			330
X				X	X	340
X				X		350
X					X	360
X						370
	X	X	X	X	X	400
	X	X	X	X		410
	X	X	X		X	420
	X	X	X			430
	X	X		X	X	440
	X	X		X		450
	X	X			X	460
	X	X				470
	X		X	X	X	500
	X		X	X		510
	X		X		X	520
	X		X			530
	X			X	X	540
	X			X		550
	X				X	560
	X					570

NOTES: 1. X means remove jumper (cut)
2. Cut only the jumpers shown. Leave the NPR jumper installed.

8. The M7277 module, located in slot 04, contains the address selection logic. The following jumper cut table indicates which jumpers should be cut to get the addresses indicated.

Jumper					Device Address
8	7	6	5	4	
		None			160000
				X	160020
			X		160040
			X	X	160060
		X			160100
		X		X	160120
		X	X		160140
		X	X	X	160160
	X				160200
	X			X	160220
	X		X		160240
	X		X	X	160260
	X	X			160300
	X	X		X	160320
	X	X	X		160340
	X	X	X	X	160360
X					160400
X				X	160420
X			X		160440
X			X	X	160460
X		X			160500
X		X		X	160520
X		X	X		160540
X		X	X	X	160560
X	X				160600
X	X			X	160620
X	X		X		160640
X	X		X	X	160660
X	X	X			160700
X	X	X		X	160720
X	X	X	X		160740
X	X	X	X	X	160760
					. . .

NOTE: X means remove jumper (cut).

The numbers identifying the jumpers are located on the M7277 etch right underneath the jumpers. In the set of five jumpers located near the center of the board, the order from top to bottom is: 8-11-12-10-9. In the set of four jumpers located near the edge of the board, the order from top to bottom is: 7-4-5-6.

9. Measure the resistance between the following pins on the backplane with the white plugs of the 7009561 cable hanging free (not plugged in):

   +5 V to GND must be 0.4 ohm to 10 ohms
   -15 V to GND must be 50 ohms to 500 ohms
   +15 V to GND must be 50 ohms to 500 ohms

   If the resistance is less than the lower limit indicated, check for a short. If the resistance exceeds the high limit, it may indicate an open circuit. Measure the resistance using the X1 scale. For the first measurement, place the red (+) probe on the +5 V terminal and the (-) lead on the GND terminal. In the second measurement, place the red (+) probe on the -15 V terminal and the black (-) lead on the GND terminal. For the third measurement, place the red (+) probe on the +15 V terminal and the black (-) lead on the GND terminal. If the above resistances are OK, connect the white plugs in accordance with D-UA-DH11-0-0.

10. Install the 7008456 Distribution Panel as indicated in D-UA-DH11-0-0 for the DH11-AA or AC. Be sure to install the module restraining bar across the back to hold the modules in case of cable strain. If installing a DH11-AD or AE panel, go to step 14.

11. Install the H758 or H739 Power Supply as shown in D-UA-DH11-0-0. Make sure the toggle switch is in the OFF position. Check the fuse with an ohmmeter. Plug the power plug into the receptacle strip on the cabinet or other processor switched outlet. Position the 7008493 Power Harness by running it up to the top of the cabinet, forward, then down to the distribution panel terminals. It is necessary to gain side access to do this. Mount the H758 on the rack. Do not mount the H758 on the door; you will be unable to close the door. The H739 can be mounted on the door. Be careful that the Faston tabs on the end of the distribution panel do not touch the frame.

12. Install an M971 cable module at each end of the BC08S cable and install the M971s thus equipped in the locations indicated in the D-MU-DH11-0-3 module utilization for the basic logic and in the D-MU-DM11-A-3 module utilization for the distribution panel. These are locations B07 in the DH11 and B01 in the distribution panel.

13. Install the M974 Maintenance Card in location B03 of the distribution panel. Be sure to remove it before starting the on-line tests. If installing the DH11-AA, AB, or AC, go to step 19.

14. For DH11-AD and AEs, install the H317-B EIA distribution panel assembly as indicated in D-UA-DH11-0-0.

15. For DH11-AD or AE installation, refer to Figure 2-3 for cable interconnections and to Figure 2-5 for proper insertion of the BC08S cables. These cables connect the data lines to the distribution panel and should not be installed until after all the off-line tests have run. The M5906 module should have H8611 test connectors in plugs J1 and J2.

CAUTION

Cables are neither marked nor keyed and if improperly connected can damage equipment. On the H317, the rib side of the cable must be away from the board. On the M5906 the smooth side of the cable must be away from the board.

16. The H317-B EIA Distribution Panel provides for several jumper selections (Figures 2-6 and 2-7). The DTR and REQUEST TO SEND leads (Figure 2-6) are normally strapped to a positive ON voltage for the DH11-AE. This strapping must be removed for lines that use a full modem control arrangement in which the modem control signals are combined with the data signals on the distribution panel. This is the case when modem control is used with the DH11-AD.

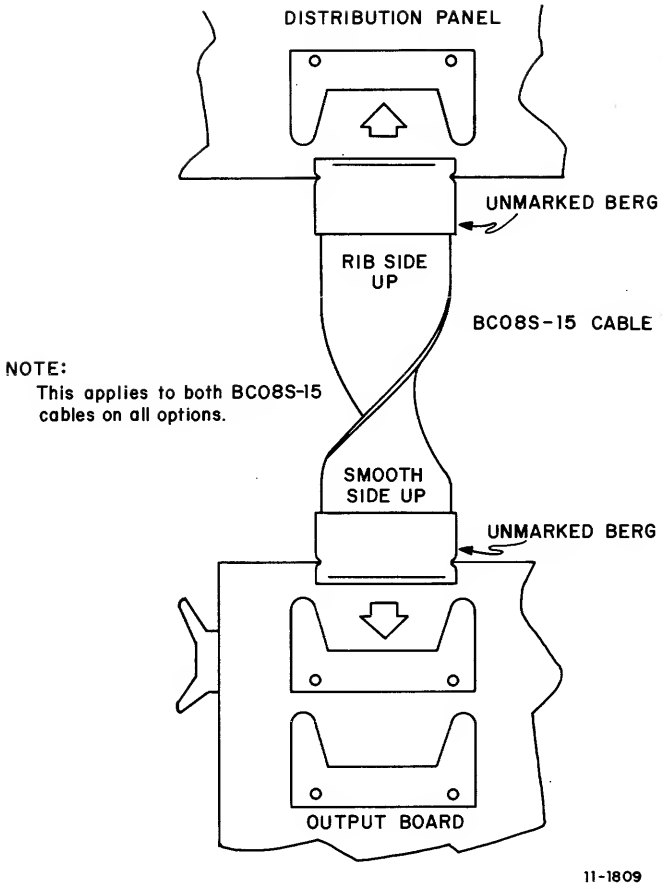


Figure 2-5 BC08S-15 Cable Polarization Diagram

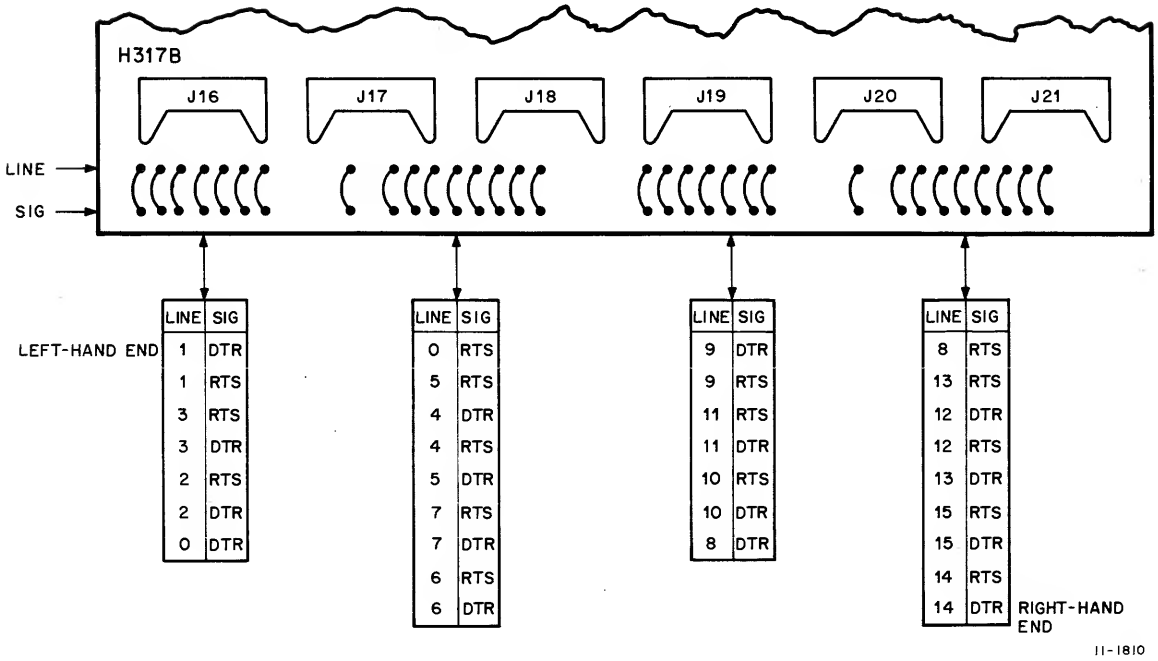
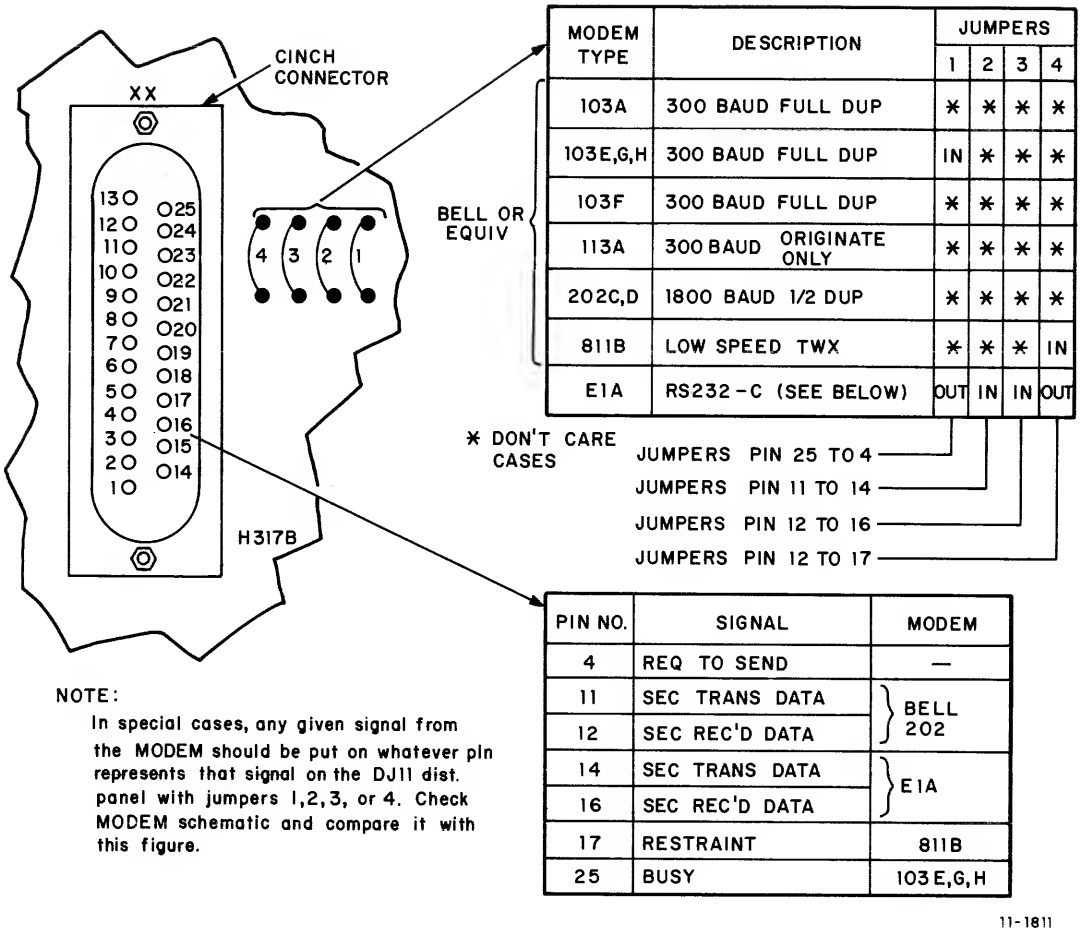


Figure 2-6 Strapping on H317B Distribution Panel



MODEM TYPE	DESCRIPTION	JUMPERS 1	2	3	4
103A	300 BAUD FULL DUP	*	*	*	*
103E,G,H	300 BAUD FULL DUP	IN	*	*	*
103F	300 BAUD FULL DUP	*	*	*	*
113A	300 BAUD ORIGINATE ONLY	*	*	*	*
202C,D	1800 BAUD 1/2 DUP	*	*	*	*
811B	LOW SPEED TWX	*	*	*	IN
E1A	RS232-C (SEE BELOW)	OUT	IN	IN	OUT

PIN NO.	SIGNAL	MODEM
4	REQ TO SEND	—
11	SEC TRANS DATA	BELL 202
12	SEC REC'D DATA	BELL 202
14	SEC TRANS DATA	E1A
16	SEC REC'D DATA	E1A
17	RESTRAINT	811B
25	BUSY	103E,G,H

Figure 2-7 Cinch-Connector Strapping on H317B Distribution Panel

17. The customer may implement the following options when installing the modem control into the DH11-AD.

    a. A null modem (H312A) may be connected to a line.

    b. Bus initialization of the modem control modules (M7807 and M7808) can be inhibited by removing DH11 backpanel wire F02B2 to ground.

    c. Interrupts for all lines may be inhibited for CARRIER, RING, SEC RX, or CLEAR TO SEND by removing the wires listed below:

Status	DH11 Wire Removed
CARRIER	E02A1 to D02B1
RING	E02C1 to D02F2
SEC RX	E02B1 to D02A1
CLEAR TO SEND	E02D1 to D02C1

18. Figure 2-8 is a wire location diagram for the DH11-AD, AE to assist in the troubleshooting of individual lines up to the outputs on the distribution panel.

19. Turn on the power. Toggle in the Bootstrap and load the Absolute Loader, if not already done. The addresses and contents of the Bootstrap Loader are listed below.

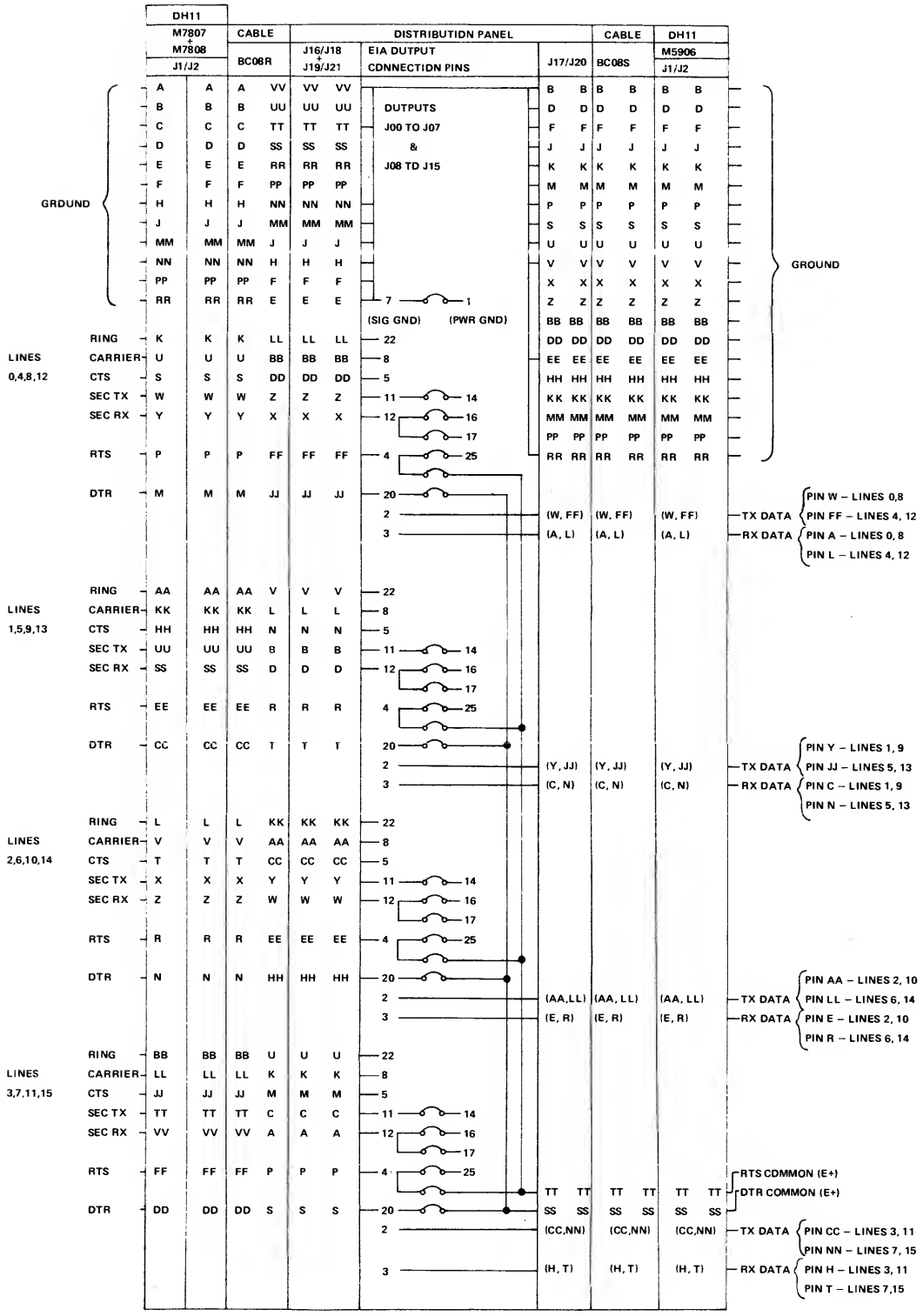
NOTE
Memory size determines the first three digits

017 for 4K
037 for 8K
057 for 12K
077 for 16K
117 for 20K
137 for 24K
157 for 28K

Address	Contents
–744	016 701
–746	000 026
–750	012 702
–752	000 352
–754	005 211
–756	105 711
–760	100 376
–762	116 162
–764	000 002
–766	– 400
–770	005 267
–772	177 756
–774	000 765
–776	177 560 (keyboard) or 177 550 (high speed reader)

20. Run the diagnostics in accordance with the instructions contained therein. Helpful information may be found in the DH11 Module Test Procedure, A-SP-DH11-0-11. One course of action not mentioned in the procedure is worthy of attention: if a diagnostic does not run, try a couple of other diagnostics before assuming that the diagnostic tape is no good. If both DZDHG and DZDHH run, the DH11 is operational; however, all diagnostics are important and should be run.

21. Run the On-Line Test, DZDHJ, in accordance with the instructions therein. Be sure to remove the M974 from the distribution panel.



NOTES: 1. M7807 – LINES 8 TO 15: J1–8 TO 11; J2–12 TO 15

2. M7808 – LINES 0 TO 7: J1–0 TO 3; J2–4 TO 7

3. DISTRIBUTION PANEL (16 LINES) J16–0 TO 3, J18–4 TO 7, J17–0 TO 7 (CONTROL); J19–8 TO 11, J21–12 TO 15, J20–8 TO 15 (DATA)

4. M5906 (16 DATA LINES) J1–8 TO 15; J2–0 TO 7

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Figure 2-8 DH11-AD, AE Wire Location Diagram

CHAPTER 3
PROGRAMMING

3.1 INTRODUCTION

This chapter contains general DH11 programming information. It is divided into two sections; one lists the bit assignments and functions of the eight registers and the other discusses several DH11 operational features and programming constraints.

3.2 REGISTER BIT ASSIGNMENTS

3.2.1 System Control Register

The System Control Register is a byte-addressable register. The register format is shown in Figure 3-1.

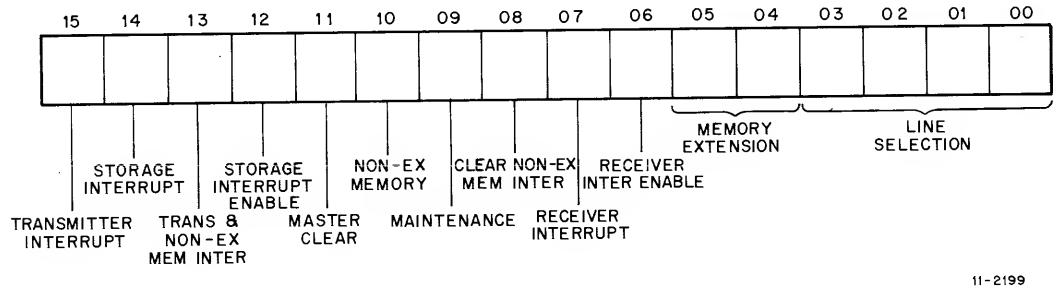


Figure 3-1 System Control Register Format

Bit	Function
00, 01, 02, 03	Line Selection – Each of the 16 lines served by the DH11 has its own storage for line parameter information, current address, and byte count. These storage locations are loaded by the program via the Line Parameter Register, Current Address Register, and Byte Count Register, but the hardware must first be told which line is to have its line parameters, current address, or byte count changed. This routine is accomplished by setting the line selection bits. These bits are read/write.

Bit	Function
04, 05	Memory Extension – The information stored in these bits becomes bits 16 and 17, respectively, of any current address loaded by the program into the Current Address Register. These bits are read/write, but when read, represent only the status of bits 4 and 5 of the System Control Register, not the status of the 16th and 17th address bits of the selected line. (See Paragraph 3.2.8 for further information.) The reason for this arrangement is to permit interrupt service routines to save the contents of the System Control Register accurately.
06	Receiver Interrupt Enable – This bit, when set, enables receiver interrupts (bit 07).
07	Receiver Interrupt – This bit, when set, indicates that the number of characters stored in the silo exceeds the alarm level specified by the low byte of the Silo Status Register. This bit is read only, except in maintenance mode, when it is read/write. When set, this bit generates an interrupt if bit 06 is also set.
08	Clear Non-Existent Memory Interrupt – This bit, when set, clears the non-existent memory interrupt flip-flop (bit 10) and clears itself. This bit is read/write.
09	Maintenance (Read/Write) – This bit, when set, places the DH11 in maintenance mode.
10	Non-Existent Memory – This bit is set whenever the NPR hardware within the DH11 addresses a memory location from which no slave sync signal is received within 20 μs. This indicates that the addressed location or device does not exist. This bit causes an interrupt if bit 13 is set also. This bit is read-only, unless in maintenance mode, at which time it is read/write.
11	Master Clear – This bit, when set, generates the initialize condition within the DH11, clearing the silo, UARTs, and registers. This bit is read/write.
12	Storage Interrupt Enable – This bit, when set, permits the setting of bit 14 to generate an interrupt. This bit is read/write.
13	Transmit and Non-Ex-Mem Interrupt Enable – This bit, when set, permits the setting of bit 10 or 15 to generate an interrupt. This bit is read/write.
14	Storage Interrupt – This bit is set whenever the receiver scanner has found a receiver holding buffer with a character in it and desires to store that character in the silo but cannot do so at this time because of a lack of space. When set, this bit causes an interrupt if bit 12 is set. This bit is read-only, except in maintenance mode, at which time it is read/write.

Bit	Function
15	Transmitter Interrupt – This bit is set whenever the DH11 concludes an NPR cycle that incremented a byte count to 0, indicating the loading of the last character in a message buffer into a UART transmitter holding register. This bit, when set, causes an interrupt if bit 13 is set. This bit is read/write. It is set during an NPR cycle so no hardware/software synchronizing problems occur.

3.2.2 Next Received Character Register

The Next Received Character Register is read-only and is word addressable. The register format is shown in Figure 3-2.

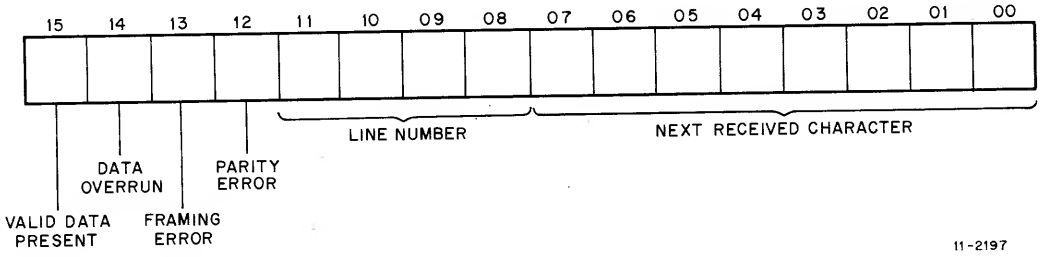


Figure 3-2 Next Received Character Register Format

Bit		Function
00 – 07	00 – 07	These bits contain the next received character, right justified. The least significant bit is bit 00. Unused bits are 0. The parity bit is not shown.
	08 – 11	These bits contain the line number upon which the character was received. Bit 08 is the least significant.
	12	Parity Error – This bit is set if the sense of the parity of the received character does not agree with that designated for that line.
	13	Framing Error – This bit is set if the received character did not have a stop bit present at the proper time. This bit is usually interpreted as indicating the reception of a break.
	14	Data Overrun – This bit is set if the received character is preceded by a character that was lost due to the inability of the receiver scanner to service the UART receiver holding buffer.
	15	Valid Data Present – This bit indicates that the data presented in bits 14 – 00 is valid. It permits the use of a character handling program that takes characters from the silo until there are no more available. This is done by reading this register and checking bit 15 until one obtains a word for which bit 15 is 0.

3.2.3 Line Parameter Register

This register should be loaded only after the System Control Register has had its line selection bits arranged to select the line to which these line parameters are to apply. The register format is shown in Figure 3-3. This register is write-only.

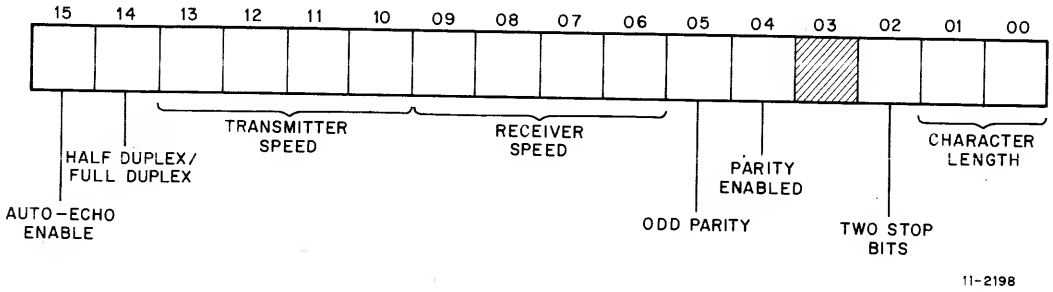


Figure 3-3 Line Parameter Register Format

Bit	Function
00 – 01	Character Length – These bits are set to receive and transmit characters of the length (excluding parity) shown below.

01	00	Bit
0	0	5 bit
0	1	6 bit
1	0	7 bit
1	1	8 bit

02	Two Stop Bits – This bit, when set, conditions a line transmitting with 6, 7, or 8 bit code to transmit characters having two stop marks. If the line is transmitting 5 bit code, assertion of this bit causes the characters to be transmitted with 1.5 stop marks. If this bit is not asserted, 1 stop mark is sent.
03	Reserved (Not used)
04	Parity Enabled – If this bit is set, characters transmitted on the line have an appropriate parity bit affixed, and characters received on the line have their parity checked.
05	Odd Parity – If this bit and bit 4 are set, characters of odd parity are generated on the line and incoming characters are expected to have odd parity. If this bit is not set, but bit 4 is set, characters of even parity are generated on the line and incoming characters are expected to have even parity. If bit 4 is not set, the setting of this bit is immaterial.

Bit	Function
06 – 09	Receiver Speed – The state of these bits determines the operating speed for the receiver of the selected line. The speed table below is applicable.
10 – 13	Transmitter Speed – The state of these bits determines the operating speed for the transmitter of the selected line. The speed table below is applicable.

Speed Table for Receiver and Transmitter Speeds

9	8	7	6	(Receiver bits)
13	12	11	10	(Transmitter bits)
0	0	0	0	Zero Baud
0	0	0	1	50 Baud
0	0	1	0	75 Baud
0	0	1	1	110 Baud
0	1	0	0	134.5 Baud
0	1	0	1	150 Baud
0	1	1	0	200 Baud
0	1	1	1	300 Baud
1	0	0	0	600 Baud
1	0	0	1	1200 Baud
1	0	1	0	1800 Baud
1	0	1	1	2400 Baud
1	1	0	0	4800 Baud
1	1	0	1	9600 Baud
1	1	1	0	External Input A
1	1	1	1	External Input B

14	Half Duplex/Full Duplex – If this bit is set, the line is conditioned to operate in half-duplex mode. If this bit is clear, the line is conditioned to operate in full-duplex mode. In this application half duplex means that the DH11 receiver is blinded during transmission of a character.
15	Auto-Echo Enable – When this bit is set, characters received on the line are to be hardware echoed.

3.2.4 Current Address Register

This register should be loaded only after the System Control Register has had the appropriate bits set to select the line number to which this current address is to apply. When this register is loaded, address bits 00 – 15 are transferred into semiconductor memories in the DH11 from bits 00 – 15, respectively, of this register. Address bits 16 – 17 are transferred into semiconductor memories in the DH11 from bits 4 – 5 of the System Control Register.

When this register is read, it indicates the current address of the line selected by the System Control Register. Bits 16 and 17 appear in the Silo Status Register.

3.2.5 Byte Count Register

In the same fashion as the Line Parameter and Current Address Registers, this register should not be loaded or read without first selecting a line number by means of the lower order four bits of the System Control Register. This register should be loaded with the 2's complement of the number of characters (bytes) to be transmitted on that line. Thc Byte Count Register is read/write.

3.2.6 Buffer Active Register

This register contains one bit for each line. The bits are set individually. using BIS instructions. Setting a bit initiates transmission on the associated line. The bit is cleared by the hardware when the last character to be transmitted on that line is loaded into the transmitter Data Holding Register of the UART for that line. It should be noted that while the clearing of a BAR bit does indicate that a new message may be sent, it does not indicate that the last characters from the preceding message have been completely sent. Specifically, two more characters are sent after the BAR bit clears. These are the last two characters of the message; one of them is starting when the BAR is cleared, and one is the final character loaded into the holding register, thus clearing the BAR bit. This effect is a normal consequence of double-buffered transmission and is mentioned here for the benefit of programmers who want to write programs that control such modem leads as Request To Send. Clearly, Request To Send should not be dropped until at least two character times after the BAR bit for a given line clears.

Clearing a BAR bit should not be used to abort transmission on a line. Rather, the byte count for that line should be sent to 0. In this way, a transmitter interrupt is generated. The Buffer Active Register bits are read/write.

3.2.7 Break Control Register

This register contains one bit for each line. Setting a bit in this register immediately generates a break condition on the line corresponding to that bit number; clearing the bit terminates the break condition. The break condition may be timed by sending characters during the break interval, since these characters never actually reach the line.

3.2.8 Silo Status Register

This register is actually two byte-sized registers. The register format is shown in Figure 3-4.

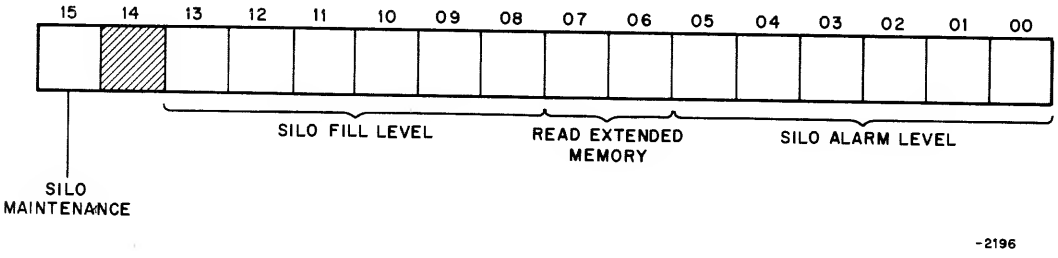


Figure 3-4 Silo Status Register Format

Bit	Function
00 – 05	Silo Alarm Level – The program writes a number corresponding to the desired silo alarm level into this location (see Paragraph 3.3.4, Silo, for programming considerations). When the number of characters stored in the silo exceeds that number, an interrupt (System Control Register bit 7) is generated, if enabled (System Control Register bit 6 is 1). These bits are read/write.

Bit	Function
06 – 07	Read Extended Memory – These bits are read-only and contain the A16 and A17 bits of the current address for the line to which the line selection bits of the System Control Register are pointing.
08 – 13	Silo Fill Level – These bits represent an up-down counter that indicates the actual number of characters in the silo. It should be noted that there are six binary digits; hence numbers between 0 and 63_{10} can be represented. A full silo has 64_{10} entries and appears as 00000, but one may easily tell the difference between an empty silo (00000) and a full silo (00000) by checking the storage overflow bit (bit 14 of the System Control Register). These bits are read-oniy.
14	Reserved
15	Silo Maintenance – Each time this bit is set, a fixed binary pattern (1010101010101010) is sent to the silo once for checking during maintenance. Clearing and setting loads another copy of the pattern.

3.3 OPERATIONAL FEATURES WITH PROGRAMMING SIGNIFICANCE

3.3.1 Introduction

This section includes the discussion of several operational features of the DH11 that have programming significance. The discussion covers the DH11 device and vector address requirements, the double-buffered feature of the UARTs, operation of the silo, use of break signals, and the function of the maintenance bits.

3.3.2 Floating Device and Vector Addresses

The DH11 uses floating device addresses that are located after the DJ11s in the floating address space that begins at location 160010. Because the DH11 has eight registers, it must be assigned an address that is a multiple of 20 (octal). All DH11s in a system should have consecutive addresses.

Example 1: A system with no DJ11s, but two DH11s:

160010 Cannot use for DH11s because not multiple of 20.
160020 First DH11
160040 Second DH11
160060 DH11 gap (indicates that there are no more DH11s).

Example 2: A system with one DJ11, two DH11s:

160010 First DJ11
160020 DJ11 gap (indicates that there are no more DJ11s).
160030 Cannot use for DH11s because not multiple of 20.
160040 First DH11
160060 Second DH11
160100 DH11 gap (indicates that there are no more DH11s).

The DH11 requires two vector addresses which follow those of the DJ11 in the floating vector space that starts at address 300. The vectors starting at 300 are used in the following order: DC11; KL11/DL11-A,B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C,D,E; DJ11; DH11.

Of the two DH11 vectors, the receiver vector is the lower numbered vector. The priority of the receiver and transmitter interrupts are individually selectable by means of two standard PDP-11 priority jumper plugs.

3.3.3 Double-Buffered Receivers and Transmitters

The receiver and transmitter sections of the UART are double-buffered; that is, each section contains a Shift Register and a Holding Register. For the receiver, the serial input character goes to the Shift Register which performs a serial-to-parallel conversion and transfers the character in parallel to the Holding Register. At this point, the DA (Received Data Available) flag goes high. In the DH11, the DA flags of the 16 UARTs are sampled by the receiver scanner. If the scanner finds a high DA flag, it copies the data from the receiver Holding Register into the silo, if space is available. If space is not available, the Storage Interrupt bit in the CSR is set and a receiver interrupt is generated, if enabled. This does not mean that the data has been lost. Rather, it indicates that the data in this or any other receiver Holding Register will be lost if the scanner cannot move the data to the silo before an additional character arrives on the line. Actual data loss is apparent to the program when characters are received with the DATA OVERRUN bit set.

For the transmitter, the Holding Register can be loaded in parallel with a character to be transmitted when the TBMT (Transmitter Buffer Empty) flag goes high. The character is automatically transferred to the Shift Register when this register becomes empty. The desired start, stop, and parity bits are added to the character and serial transmission begins. At the end of a character transmission, the EOC (End of Character) flag goes high and remains in this state until transmission of a new character begins.

3.3.4 Silo

The silo, actually more similar in design to a grainery, is a first-in, first-out buffer store. A parallel loaded 16-bit word (see Paragraph 3.2.2 for the format) automatically propagates downward into the first location not already containing a word. When the silo is empty, the word propagates directly into the Next Received Character Register. The propagation time from the top of the silo to the bottom may be as much as 32 μs. For this reason, the hardware is arranged such that the receiver interrupt is not generated until the number of characters in the silo exceeds the silo alarm level and there is at least one character in the bottom of the silo. This arrangement is necessary because the up-down counter that indicates the number of characters in the silo indicates exactly that: the number of characters in the silo, which includes those resting in the bottom and those propagating downward.

While the hardware arrangement protects the case where the silo is empty and the alarm level is zero, the number of characters in the silo and the number actually available to be serviced may differ due to the propagation time. If having at least one character in the bottom of the silo was not made a condition in the interrupt generation, the program would receive an interrupt while the single character in the silo was propagating downward. For this reason, character handling programs should not assume there are some particular number of characters in the silo when servicing begins. Rather, the program should extract a character, check the valid data present bit (bit 15) and handle the character; then the program should extract the next character and repeat the process until bit 15 no longer tests as a 1. At that time, the silo may be assumed to be empty (although there may be another character propagating downward) and the character handling routine may be terminated until another receiver interrupt is received.

On very fast processors, such as the PDP-11/45, the program should avoid reading the Next Received Character Register more often than once per μs, as it takes one μs for characters in the silo to shift downward one position. Since the typical program checks bit 15 and moves the character to some location, it is anticipated that this speed requirement will not pose a problem.

The silo alarm level can be set to any number from 0 through 63. However, care should be taken that an appropriate alarm level be chosen to suit software/hardware timing and system throughput requirements. At any silo alarm level, once the program enters the receive interrupt routine it is best to read all words from the NRC, checking bit 15 of each one, until a word is encountered with bit 15 equal to a zero. This implies that the silo is empty, and will maximize the usefulness of the silo alarm feature.

The programmer must be aware that new characters may enter the silo as it is being emptied, so that the silo alarm level is not meant to indicate the exact silo fill level except at the moment it interrupts. It is recommended that the receiver interrupt service routine which reads the NRC be run at a priority level equal to or higher than that of the DH11. If the receiver is able to interrupt its own service routine while the silo is being emptied, extra interrupts will be generated due to interaction of incoming data, the silo fill level, and the silo alarm level.

3.3.5 Zero Baud

A speed selection of 0 Baud is provided so that the program may turn off any line. This is useful should excessive circuit noise on an unused line cause the receipt of annoying quantities of bogus characters.

3.3.6 Break Signals

When the Break Control Register has been conditioned to transmit a break signal on a particular line, DH11 logic immediately forces the output on that line to the space (0) condition.

The generation of a transmitter interrupt occurs when the last character of a message has been loaded into a UART transmitter from a message table in the PDP-11 memory. It is thus appropriate at that time for the program to set up a new message in memory and to load the appropriate current address and byte count so that the new message can begin when the old one is finished.

It is important to note that the former message is not finished when the transmitter interrupt is given; rather, the use of the memory table is finished. In terms of the actual serial communications line, there are two more characters left to go. One of these characters is in the UART transmitter's Shift Register; the other is in the UART transmitter's Holding Register.

The consequence of the above condition is that to send a break signal, one should load two nulls (all ones) and wait for a transmitter interrupt before setting the appropriate bit in the Break Control Register. In this way, generation of a break does not interrupt the transmission of any printing characters. In like manner, when using characters to time the transmission of a break signal, nulls should be used so that when the break condition is terminated by clearing the bit in the Break Control Register, no printing characters are produced from the UART Shift and Holding Registers.

3.3.7 Initialize Signal

The Initialize signal clears the silo, UARTs, and all registers except the Current Address and Byte Count Registers. All scanners are forced to line 00 but continue operation from there.

3.3.8 Maintenance Bits SCR 09 and SSR 15

Setting bit SCR 09 (Maintenance) causes the following action:

> Enables the ability of the program to write SCR 07 (Receiver Interrupt), SCR 10 (Non-Existent Memory Interrupt), and SCR 14 (Storage Overflow Interrupt) bits. This write capability is normally not enabled as it can produce hardware/software synchronization problems unless carefully done.

The following precaution must be observed in the maintenance mode. If the program reads bit 7 of the SCR and finds that it is a 1, the program must perform a Bit Clear instruction on bit 7 before reading the NRC. This is required because in the maintenance mode, bit 7 is an OR function of the output of a program-controlled flip-flop and a signal from the silo alarm circuit. If SCR bit 7 is read, and is found to be a 1, and the Bit Clear instruction is not performed, the flip-flop is set during the restore portion of the Unibus read cycle. Because of the OR function, the flip-flop masks the transitions of the silo alarm circuit that occurs when the NRC is read. These transitions are required for proper operation of the M7821 Interrupt Module.

Loops the transmitted data leads (serial out line 00 – 15) to the received data leads (serial in line 00 – 15).

Setting bit SSR 15 (Silo Maintenance) causes the inputs of the silo to be set to a 1010101010101010 bit pattern, and a single 16-bit character made up of this pattern to be loaded into the silo. Successive clears and sets of SSR 15 repeat this procedure. All receiver speeds should be set to 0 Baud and the silo emptied before this is done, so that no data from the incoming serial lines is placed in the silo while it is under test.

CHAPTER 4
DETAILED DESCRIPTION

4.1 INTRODUCTION

This chapter provides a detailed description of the DH11 logic. The discussion is keyed to the DH11 print set that is supplied as a separate bound volume. Additional illustrations are included in the discussion which is divided into 11 parts.

Discussion	Paragraph
Address Selector and Gating Control	4.2
Clock Module M4540	4.3
Line Parameter Control Module M7288	4.4
Transmitter Scanner	4.5
Current Address and Control Logic	4.6
Byte Count Register	4.7
Receiver Scanner	4.8
FIFO Buffer	4.9
System Control Register	4.10
Half/Full Duplex Control Logic	4.11
Registers and Byte Count Module M7278	4.12

4.2 ADDRESS SELECTOR AND GATING CONTROL

4.2.1 Address Assignment

Each DH11 multiplexer is assigned eight consecutive addresses that are decoded to generate control signals for enabling eight registers in the DH11.

A specific number of memory addresses in each PDP-11 system are reserved for communications devices. The space that includes the DH11 device addresses extends from 760020 – 764000 (octal designation). These locations are termed *floating addresses.* The conventions used for assigning floating addresses are discussed in Appendix A.

Location 760020 is assigned as the first address of the first DH11 in the system; actually, the DH11 requires eight consecutive locations (760020 – 760036). A maximum of 16 DH11s are allowed per system. The addressing space for the maximum number of DH11s is shown below, assuming that the system contains no DJ11s.

760020	1st register of 1st DH11
760022	
760024	
760026	
760030	
760032	
760034	
760036	8th register of 1st DH11
760040	1st register of 2nd DH11
760042	
760044	
.....	
.....	
760416	8th register of 16th DH11

The address selection and gating control logic is shown in drawing D-CS-M7277-0-1, sheets 3, 4, and 5.

When the program desires to read from or write into a DH11 register, it must address the register and indicate the type of operation to be performed. This is accomplished by placing the proper binary information on Unibus address lines A(17:00) and Unibus control lines C(01:00) and asserting BUS MSYN L. These signals are decoded by the DH11 logic to generate the enabling signal for the addressed register. This allows data from the Unibus data lines D(15:00) to be written into the register, or it allows the contents of the register to be placed (read) onto the Unibus data lines.

Bits C(01:00) and A00 are decoded to indicate the type of operation or Unibus transaction to be performed (Table 4-1). The DATIP transaction is not used with the DH11.

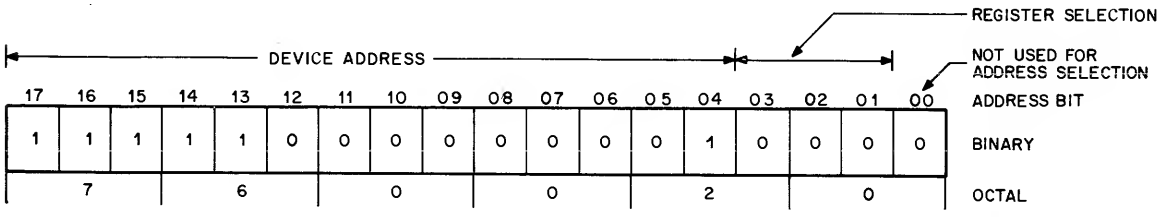
Bits A(17:04) are decoded to indicate the device address of the DH11. Each DH11 in a system has a different device address. The device address is hardwired by jumpers that are associated with bits A(12:04). Bits A(03:01) are decoded to select the desired register in the DH11.

Table 4-1
Unibus Transactions for DH11

Name	Mnemonic	C Bits		Bit A00	Function
		C01	C00		
Data In	DATI	0	0	X*	Data transmitted from DH11 to processor on D(15:00). When DH11 is master, data is transmitted in bytes from memory to DH11. Bit A00 = 0 gives low order byte. Bit A00 = 1 gives high order byte.
Data Out	DATO	1	0	X	Data transmitted from processor to DH11 on D(15:00).
Data Out, Byte	DATOB	1	1	0	Data transmitted from processor to DH11 on D(07:00) which is low byte.
		1	1	1	Data transmitted from processor to DH11 on D(15:08) which is high byte.

*X = irrelevant

The address format is shown in Figure 4-1. The example used is 760020, which is the address of the first designated register in the first DH11 installed in the system. The binary representations of the two least significant octal digits of all eight registers are shown to illustrate how device address bits A(17:04) remain unchanged and bits A(03:01) change for each register.



REGISTER NO.	REGISTER ADDRESS	ADDRESS BITS 05 04 03 02 01 00
1	760020	010000
2	760022	010010
3	760024	010100
4	760026	010110
5	760030	011000
6	760032	011010
7	760034	011100
8	760036	011110

Figure 4-1 Address Word Format

4.2.2 Device Decoding

Unibus address bits A(17:04) are used to specify the device address. They are sent from the Unibus to type 380 Unibus receivers which are 2-input NOR gates (drawing D-CS-M7277-0-1, sheet 4). They are shown as logically equivalent negated-input AND gates. Twelve receivers are used for bits A(17:04). Bits A16 and A15 go to receiver E22 pins 11 and 12, and bits A14 and A13 go to receiver E22 pins 6 and 7. Bits A(12:04) go to individual receivers E22 (1), E15 (4), and E8 (4) and the other input of each of these receivers is connected to ground. Bit A17 is combined with BUS MSYN L in receiver E22 pins 9 and 10.

Eleven receivers are used for bits A(16:04). The output of each receiver is sent to one input of type 8242 2-input exclusive NOR gates E21 (3), E14 (4), and E7 (4). These gates are used as digital comparators. The gate output is high only when both inputs are identical (both high or both low). The 8242s have open collector outputs and all the outputs are connected together and returned to +5 V via an external resistor to form a wire-OR function. The common output is high only when all the 8242 gates produce high outputs.

Using a PDP-11 processor with a maximum limit of 64K bytes (32K words), bits A17 and A16 are forced to 1s if bits A(15:13) are all 1s when the processor is master. This allows generation of addresses 76000 – 777777 with control for only 16 address bits. This 8K byte (4K word) area is reserved for peripheral device addresses. This action relocates the last 8K addresses to the highest 8K locations accessible by the bus. See Appendix B for more details concerning this function.

To avoid confusion, the reader should be aware that the Unibus uses negative logic for all signals except BG(07:04) and NPG. The definitions of positive logic are shown below:

Negative Logic

Signal Asserted:	Low = Logical 1 = 0 V
Signal at Rest:	High = Logical 0 = +3 V

Positive Logic

Signal Asserted:	High = Logical 1 = +3 V
Signal at Rest:	Low = Logical 0 = 0 V

In this discussion, 760020 is used as the device address. Bits A(17:13) are all 1s (Figure 4-1). These bits are Unibus signals so they are all low at the inputs of their associated receivers. Bits A16 and A15 go to receiver E22 pins 11 and 12, and bits A14 and A13 to receiver E22 pins 6 and 7. Each receiver output is high and it is sent to one input of its associated 8242 comparator. The other input of each 8242 is held high by +5 V via resistor R24, and both 8242 outputs are high. Bits A(12:04) go to separate receivers, each of which has its other input grounded (low). These receivers act like inverters and apply the inverted Unibus address signal to one input of its associated 8242 comparator. The other input to each 8242 can be held high or low by installing or removing a jumper. With the jumper out, the input is held high through a connection to +5 V via a resistor. With the jumper installed, the input is dropped to ground. The jumpers are arranged to make the DH11 respond to a specific device address. With a jumper installed, the decoder responds to a 0 on the associated Unibus address line; it responds to a 1 if the jumper is out. Using the example (Figure 4-1) and remembering the negative logic convention for the Unibus, examine bits A04 and A05 (Figure 4-2). Bit A04 is a 1, which is a low on the Unibus. This puts a high on one 8242 input and the other input is high because the jumper is removed. The inputs match so the 8242 output is high. Bit A05 is a 0, which is a high on the Unibus. This puts a low on one 8242 input and the other input is low because the jumper is installed. The inputs match so the 8242 output is high.

This action is repeated for bits A(12:06), all of which have jumpers installed, so that all 11 8242 outputs are high. The DH11 device address has been successfully decoded and this high signal is sent to 4-input NAND gate E72. Another input to E72 comes from receiver E22 pin 14. One input (pin 10) of E22 is bit A17 which is low. When the processor asserts BUS MSYN L, the other input (pin 9) of E22 goes low and its output is high. Assume that the other two inputs of E72 are high. These inputs are controlled by other functions of the DH11 and will be discussed in subsequent paragraphs. With all four inputs high, the low output (pin 6) of E72 is sent to the gating control logic.

The output of E72 is also double inverted by two Unibus drivers to assert BUS SSYN L, which is the DH11's response to the processor that it has decoded the device address. The BUS SSYN L signal is inverted by E28 to produce SSYN H, which is used as an input to Unibus Master Control Module M796.

4.2.3 Gating Control Logic

The gating control logic generates the enabling signals for the eight registers and the Unibus drivers that place the data to be read on the Unibus. These enabling signals are a function of the selected register and the type of Unibus transaction desired. A prerequisite is that the device address has been properly decoded.

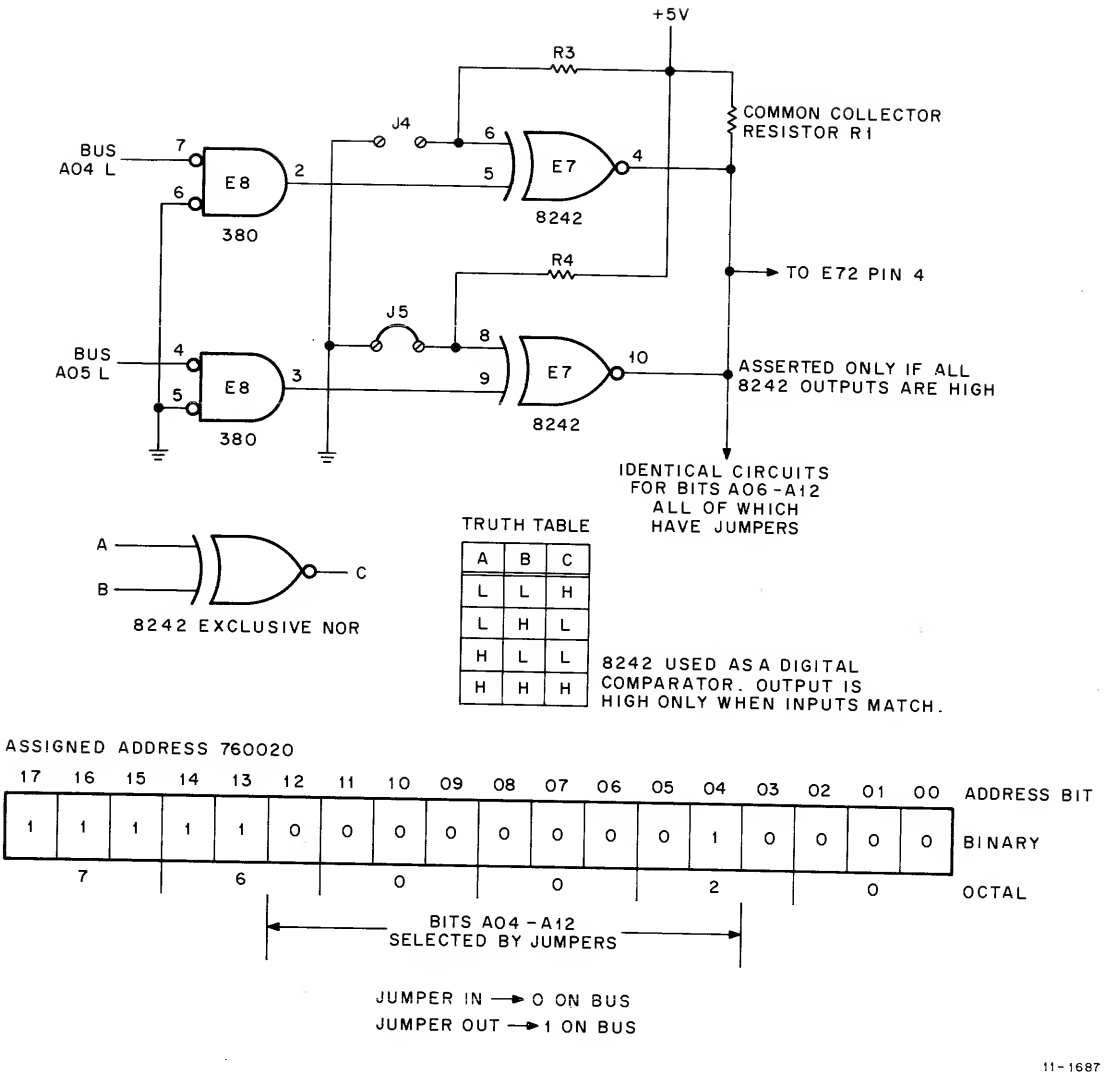


Figure 4-2 Device Address Decoding Logic

Table 4-2 lists the registers and their addresses for the example used in the discussion. Additional DH11s would be assigned different addresses but the register order remains the same.

Table 4-2
DH11 Register Address Sequence

Order	Address	Name	Type
1	760020	System Control (SCR)	Read/Write High and Low Bytes
2	760022	Next Received Character (NRC)	Read-Only
3	760024	Line Parameter (LPR)	Write-Only
4	760026	Current Address (CA)	Read/Write
5	760030	Byte Count (BC)	Read/Write
6	760032	Buffer Active (BAR)	Read/Write
7	760034	Break Control (BCR)	Read/Write
8	760036	Silo Status (SSR)	Read/Write High Byte Only

The gating control signals, or register enabling signals, are listed in Table 4-3. The signal name, source, and function are indicated. Register selection is performed by decoding bits A(03:01) and using them as the binary code to control 7442 4-line-to-10-line decoder E51. In this case, only 8 of the 10 outputs are used. Three of the four inputs (D0, D1, and D2) are used as the binary code and the fourth input (D3) is used as a strobe or enabling signal. Bit A03 goes to D2 as the most significant bit; bit A02 goes to D1 and bit A01 goes to D0. The D3 input comes from gate E72 which produces the low enabling signal when the DH11 device address is decoded and BUS MSYN L is asserted. The 7442 decoder functions as a 3-wire binary-to-octal decoder (Figure 4-3). When the strobe (D3 input) is low, the octal data is taken from outputs 0 – 7. The output of the 7442 decoder is sent to one input of the gate associated with the desired register control signal. Output 0 of the decoder goes to E34 pin 5 and E34 pin 3 to allow bytes to be written into the System Control Register. One input (pin 2) of gate E53 comes from 3-input NAND gate E55 (shown as negated-input NOR) whose inputs come from outputs 3, 4, and 7 of the 7442 decoder. These outputs represent selection of the Current Address Register, Byte Count Register, or Silo Status Register. When a read operation is desired for any of these registers, the read enabling signal is generated at E53 pin 3.

Table 4-3
Gating Control Signals

Signal	Source* (Gate Output)	Function
LOAD CA H	Gate E58 pin 13	Write into Current Address Register
LOAD BC H	Gate E69 pin 4	Write into Byte Count Register
LOAD LPR H	Gate E58 pin 1	Write into Line Parameter Register
LOAD SCR HIGH BYTE H	Gate E34 pin 4	Write into high byte of System Control Register
LOAD SCR LOW BYTE H	Gate E34 pin 1	Write into low byte of System Control Register
LOAD BAR LB or HB L	Inverter E35 pin 4	Write into low byte or high byte of Buffer Active Register
LOAD SSR LOW BYTE H	Gate E34 pin 13	Write into low byte of Silo Status Register
LOAD SSR HIGH BYTE H	Gate E34 pin 10	Write into high byte of Silo Status Register
LOAD BCR H	Gate E69 pin 13	Write into Break Control Register
READ CA or BC or SSR L	Gate E53 pin 3	Read Current Address Register, Byte Count Register, or Silo Status Register
READ NRC H	Gate E58 pin 4	Read Next Received Character Register
DATA TO BUS H	Gate E58 pin 10	Enable Unibus drivers

*All gates are shown on drawing D-CS-M7277-0-1, sheet 4.

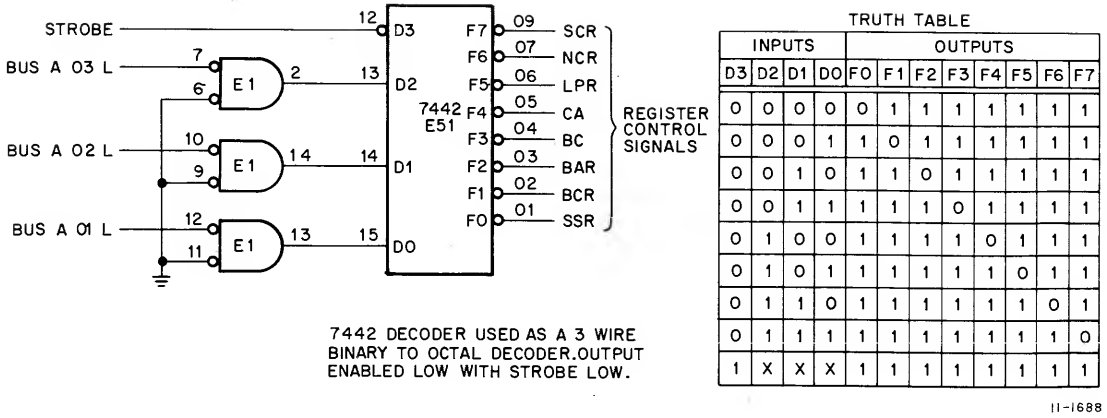


Figure 4-3 Selection of Register Gating Signals

The other input of each register selection gate is qualified as a function of the decoded Unibus transfer using bits C(01:00) and A00 (Table 4-1). The gates are qualified in groups as shown below.

Unibus Transaction	**Gates Qualified**
DATI	All READ gates plus DATA TO BUS Gate
DATO	All LOAD gates
DATOB, Low Byte	All LOAD gates except LOAD SCR HIGH BYTE and LOAD SSR HIGH BYTE gates
DATOB, High Byte	All LOAD gates except LOAD SCR LOW BYTE and LOAD SSR LOW BYTE gates

The output of gate E58 (LOAD LPR H) goes to pins 3 and 4 of type 74121 one-shot E54 (drawing D-CS-M7277-0-1, sheet 3). Pin 5 of this one-shot is held high by +3 V. Under these conditions, a negative edge at either pin 3 or 4 triggers the one-shot. Prior to triggering, the 1-output (pin 6) is low and the 0-output (pin 1) is high. When it triggers, a positive pulse is generated at the 1-output and a negative pulse is generated at the 0-output. The pulse duration is 300 ns and when it terminates, the outputs return to their original states. When LOAD LPR H is low (non-asserted) the one-shot is not triggered because its input (pins 3 and 4) reacts only to a negative edge transition. When the program desires to write into the Line Parameter Register, gate E58 pin 1 is asserted and LOAD LPR H goes high. This positive edge transition does not trigger the one-shot, but when LOAD LPR H goes low again after BUS MSYN L is cleared, a negative edge transition is generated which triggers the one-shot. The low pulse from the 0-output of the one-shot enables inputs on the type 74152 4-line to 16-line multiplexer E47 and it selects the proper line to which the line parameters are to apply. An enabling pulse of approximately 300 ns is required to ensure that the line parameters are loaded into the UARTs from the Line Parameter Register. The proper line is selected by bits 00 – 03 (SCR 00 H – SCR 03 H) from the Line Selection Register to the BCD decoding inputs of the 74154.

The 1-output of one-shot E54 is fed back to the device selection logic to prevent the DH11 from responding to another LOAD LPR or LOAD SCR instruction while the 300 ns pulse is being issued (Paragraph 4.2.4).

The outputs of the A(03:01) receivers are buffered by type 7417 non-inverting buffers and sent to the data select inputs of 16 type 74151 8-line to 1-line multiplexers shown in drawing D-CS-M7278-0-1, sheets 5, 6, 7, and 8. These signals are identified as DATA SOURCE C H, DATA SOURCE B H, and DATA SOURCE A H.

The output of the eight DH11 registers are sent to the inputs of the 16 multiplexers. During a DATI transaction, the data from the register being read is multiplexed to Unibus drivers and enabled to the Unibus by the DATA TO BUS H signal from gate E58 pin 10.

4.2.4 Address Response Inhibiting Logic

Three one-shots are used to inhibit response to an address under certain conditions.

The first condition concerns disabling the register control signals as part of the initialization process caused by setting bit 11 of the System Control Register. When the program sets bit 11 of the System Control Register, signal SCR 11 is high and is sent to pin 5 of NAND gate E53 (drawing D-CS-M7277-0-1, sheet 3). The other input of this gate becomes high when the instruction that set SCR 11 is concluded. When the output of E53 goes low, the negative transition triggers one-shot E60 and sends a negative pulse of 2.4 μs duration to pin 2 of gate E72. The output of E72 is driven high which prevents the generation of DEVICE RESPONDING L and thus prevents generation of SSYN L for the duration of the 2.4 μs initialization pulse generated by E60. In this way, the DH11 will not accept new instructions until at least 2.4 μs after the end of the initialization instruction. This allows time for the UARTs to be cleared.

The negative pulse from one-shot E60 is also sent to 4-input NAND buffer E71 and is inverted to produce INIT A H. This signal is inverted by NAND buffer E71 to produce INIT A L. It is also inverted by NAND buffer E66 to produce INIT B L. The output of this buffer is inverted to produce INIT B H. These four signals are used throughout the DH11 logic to clear the registers, UARTs, and silo.

When the program desires to perform a complete initialization of all devices on the Unibus, BUS INIT L is asserted on the Unibus. This signal is sent to pin 6 of Unibus receiver E28, is inverted, and sent also to NAND buffer E71 to generate the four Initialize signals. BUS INIT L is asserted by the PDP-11 processor during the power up sequence, during a RESET instruction, or when the processor console START switch is pressed.

The second condition concerns inhibiting response to an address for 300 ns after the previous NPR transaction has been cleared. This is accomplished by sensing the END CYCLE L signal from the M796 Unibus Master Control Module. This signal is a 100 ns pulse that is generated when certain M796 signals are cleared to indicate the end of the current NPR transaction. The leading negative edge of the END CYCLE L pulse triggers one-shot E61 and sends a negative pulse of 300 ns to pin 1 of gate E72. The address decoding logic is inhibited by this low input to E72 for the duration of the one-shot pulse. This delay ensures completion of the current operations within the DH11 incrementation of the Current Address and Byte Count Registers and occurs after every transaction in which the DH11 is master.

The third condition concerns inhibiting response to an address during the 300 ns interval that the 74154 multiplexer is enabled. This allows the UART control and data inputs to settle. When the Line Parameter Register (LPR) address is decoded and BUS MSYN L is asserted, LOAD LPR H is generated at gate E58 pin 1 and loads the information on the Unibus data lines into the LPR. The address decoder asserts BUS SSYN L and the processor clears BUS MSYN L. Signal LOAD LPR H now goes low and this negative transition triggers one-shot E54. The 1-output of one-shot E54 is sent to pin 9 of 2-input NAND gate E53 as CONTROL STROBE INHIBIT (1) H. The other input (pin 10) of E53 is also high because gate E72 is high due to BUS MSYN L being cleared. The output (pin 8) of gate E53 goes low and this negative transition fires one-shot E61 and sends a negative pulse of 300 ns duration to pin 1 of gate E72. This pulse inhibits the decoding logic for the duration of the one-shot pulse.

4.3 CLOCK MODULE M4540

4.3.1 Introduction

The M4540 Clock Module generates 16 different pulse trains that are used to control the speed of the UART receiver and transmitter. Expressed in Baud, they are: 50, 75, 100, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 3600, 4800, 7200, and 9600. All but 100, 3600, and 7200 are program selectable, using the Line Parameter

Register. The UART receiver and transmitter clocks must be 16 times the value of the desired Baud rate since the UART samples incoming data 16 times per second. The frequency in Hz of any of these 16 Baud rates is found by multiplying the Baud rate by 16. For example: 110 Baud X 16 = 1760 Hz; 2400 Baud X 16 = 38,400 Hz or 38.4 kHz.

The clock module consists of a 20.277 MHz crystal controlled oscillator whose output is divided by a series of counters to produce 16 different pulse trains.

The frequency division or count down function is performed by the following ICs:

2	74H74 High Speed D-Type Flip-Flops
1	7490 Decade Counter
4	7492 Divide-by-12 Counters
3	7493 4-Bit Binary Counters
3	74161 Synchronous 4-Bit Counters

Because of the various operating modes possible with these counters, the operation of the count down function is not obvious from an examination of the clock logic print (D-CS-M4540-0-1, sheet 2). The functional operation of each counter is discussed first and then the complete count down function is discussed with reference to the logic print.

4.3.2 Counter Functional Descriptions

4.3.2.1 General Information – The counters used in the clock are standard TTL Medium Scale Integration (MSI) devices. The symbols used on the logic print are from the DIGITAL IC Dictionary. The input/output designations within the symbols are different than those used in the manufacturers IC catalog; however, the pin numbers are the same as those shown in the IC catalog.

4.3.2.2 74H74 Flip-Flops – Two 74H74 high speed D-type flip-flops are used to divide the oscillator output by 2 and 4. These flip-flops are contained in a single package designated E04. Figure 4-4 shows the flip-flops and associated timing diagram.

The 20.277 MHz oscillator output is inverted by gate E09 and applied to the clock input of flip-flop A. Triggering occurs at a voltage level on the positive edge of the clock pulse and is not related to the transition time of the edge. The (0) output (pin 06) of the flip-flop is fed back to its D-input so that the flip-flop changes state at each positive edge of the clock pulse. This action produces complementary pulse trains at the (1) H and (0) H outputs that have a frequency of 10.138 MHz. Flip-flop A divides the oscillator frequency by 2. Flip-flop B is connected in a similar manner except that its clock input is the 10.138 MHz signal from the (0) H output (pin 6) of flip-flop B. Flip-flop B divides this signal by 2 to produce complementary 5.069 MHz signals at its 1 and 0 outputs. The clear and preset inputs of both flip-flops are disabled by connecting them to +3 V.

4.3.2.3 7490 Decade Counter – One 7490 counter is used and it is identified as E01 (Figure 4-5). Output R3 (1) provides a divide by 5 function for the input to CLK B0. A separate divide by 2 function is provided at output R0 (1) for the input to CLK 0. Inputs SET 9 and CLR are disabled by connecting them to ground.

4.3.2.4 7492 Divide by 12 Counter – Four 7492 counters are used and they are identified as E06, E10, E11, and E12 (Figure 4-6). All four are used as divide by 6 counters with a separate divide by 2 function. Simultaneous frequency divisions of 3 and 6 are provided at outputs R2 (1) and R3 (1) for the input to CLK BC. A separate divide by 2 function is provided at output R0 (1) for the input to CLK 0. Input CLR is disabled by connecting it to ground.

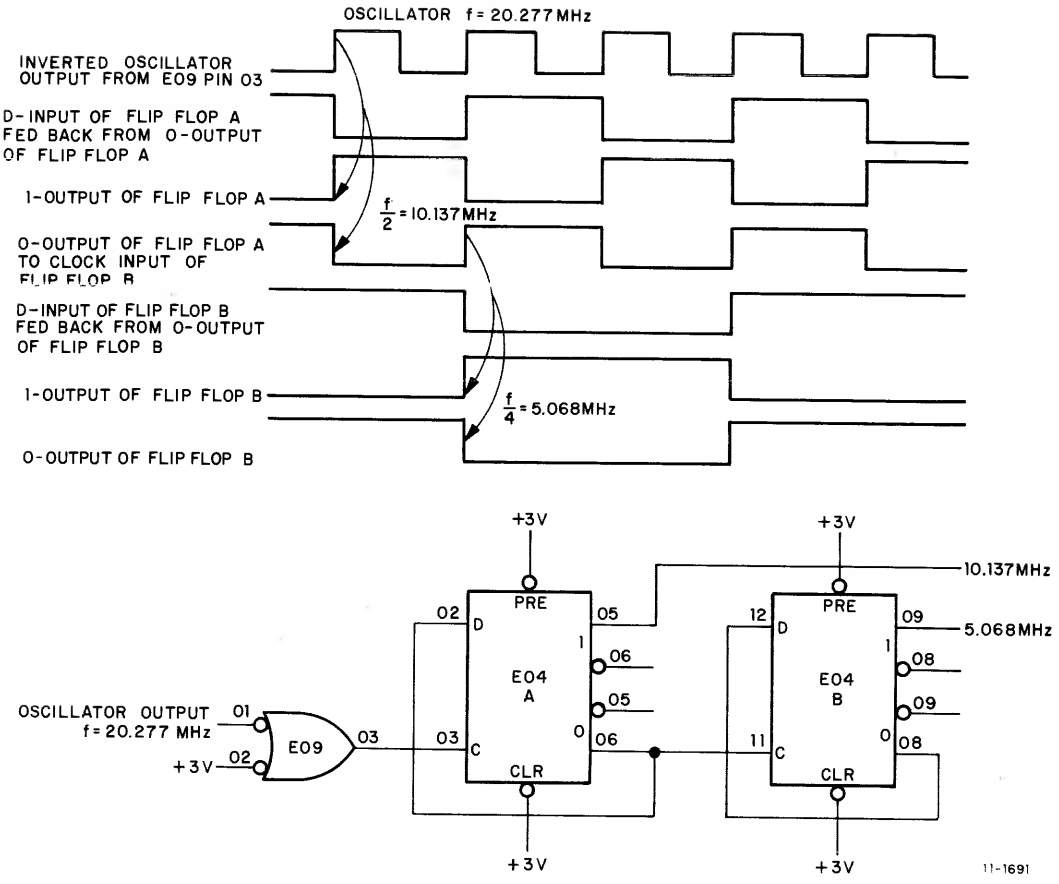


Figure 4-4 Divide Function Performed by Flip-Flop E04

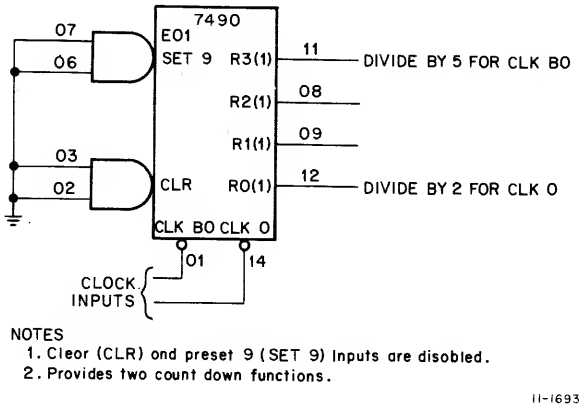


Figure 4-5 7490 Divide by 5 and Divide by 2 Counter

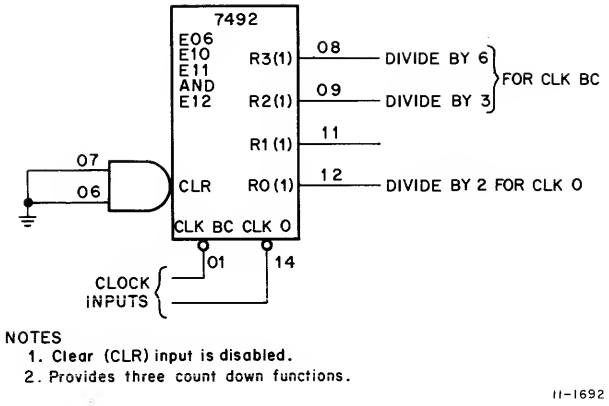


Figure 4-6 7492 Divide by 6 and Divide by 2 Counter

4.3.2.5 7493 4-Bit Binary Counter – Three 7493 counters are used and are identified as E02, E05, and E07 (Figure 4-7). One (E02) is used as a 4-bit ripple-through counter and two (E05 and E07) are used as 3-bit ripple-through counters with independent modulo 2 counters.

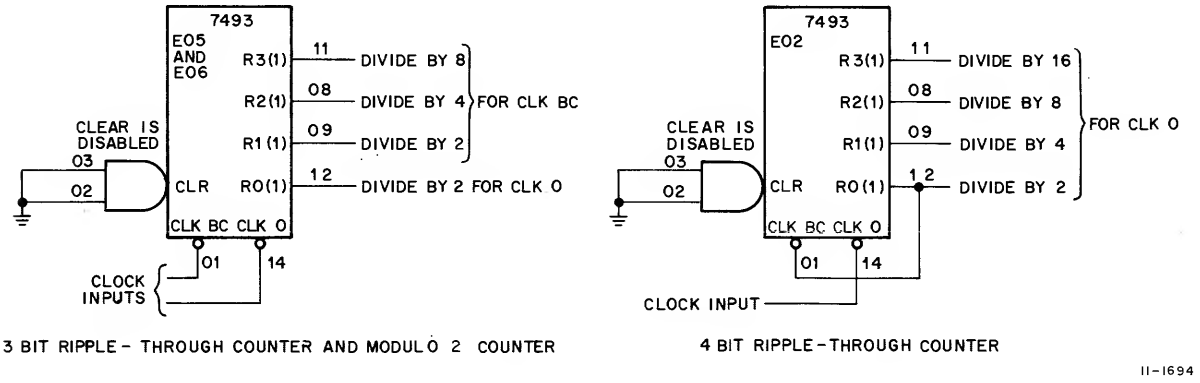


Figure 4-7 7493 4-Bit Binary Counter

In the 4-bit ripple-through configuration, output R0 (1) is connected to CLK BC and the input signal is sent to CLK 0. Simultaneous frequency divisions of 2, 4, 8, and 16 are provided at outputs R0 (1), R1 (1), R2 (1), and R3 (1) for the input to CLK 0.

In the 3-bit ripple-through configuration, no external interconnection is used. Simultaneous frequency divisions of 2, 4, and 8 are provided at outputs R1 (1), R2 (1), and R3 (1) for the input to CLK BC. A separate divide by 2 function is provided at output R0 (1) for the input to CLK 0.

In both configurations, the CLR input is disabled by connecting it to ground.

4.3.2.6 74161 Synchronous 4-Bit Counter – Three 74161 counters are used and they are identified as E03, E08, and E13 (Figure 4-8). One (E03) is preset to provide a divide by 11 function and two (E08 and E13) are preset to provide a divide by 7 function.

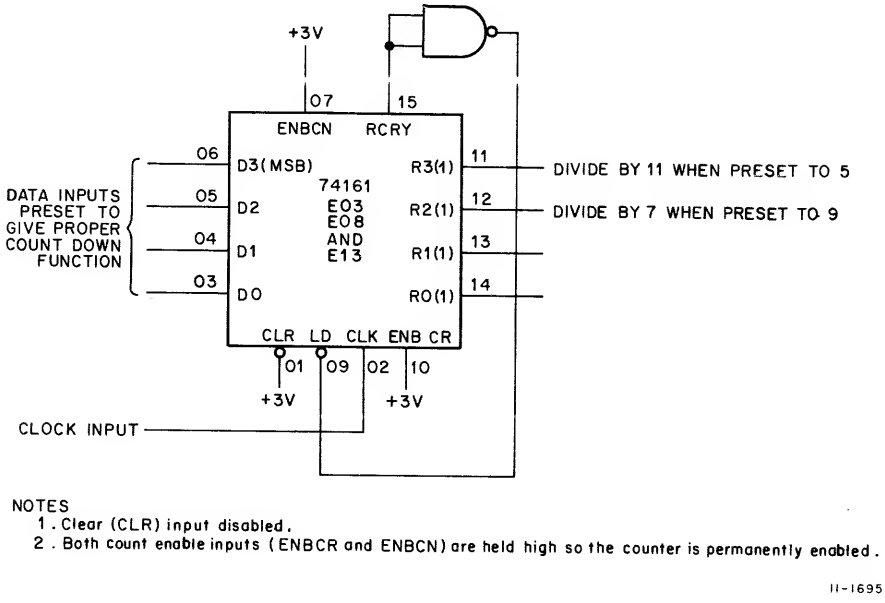


Figure 4-8 74161 Synchronous 4-Bit Counter

In both configurations, the clear (CLR) input is disabled and both count enable inputs (ENB CN and ENB CR) are held high (+3 V) so that the counter is permanently enabled. Also, the carry output (RCRY) is fed back to the load input (LD) to preset the counter on the count of 15.

To provide a divide by 11 function, inputs D3, D2, D1, and D0 are preset to the count of 5 by connecting D1 and D3 to ground (logical 0) and connecting D0 and D2 to +3 V (logical 1).

D3	D2	D1	D0	(LSB)
0	1	0	1	

The counter involved is E03 and the divide by 11 function is provided at output R3 (1) which is the most significant bit of the counter. Figure 4-9 shows a truth table and waveform for this function. The counter is preset to a count of 5 by the carry pulse that is generated on a count of 15. This high pulse is inverted by NAND gate E09 and sent to the load input (LD). A low signal to the LD input conditions the counter such that the outputs agree with the data inputs after the next pulse. Reference to Figure 4-9 shows that output R3 (1) generates a negative transition (and a positive transition) in a period equivalent to 11 input clock positive transitions. Thus, the divide by 11 function is provided at output R3 (1).

Counters E08 and E11 both provide a divide by 7 function. This is accomplished by presetting the inputs to the count of 9 and picking the signal from output R2 (1). The operation is similar to that described by the divide by 11 function. Figure 4-10 shows a truth table and waveform for the divide by 7 function.

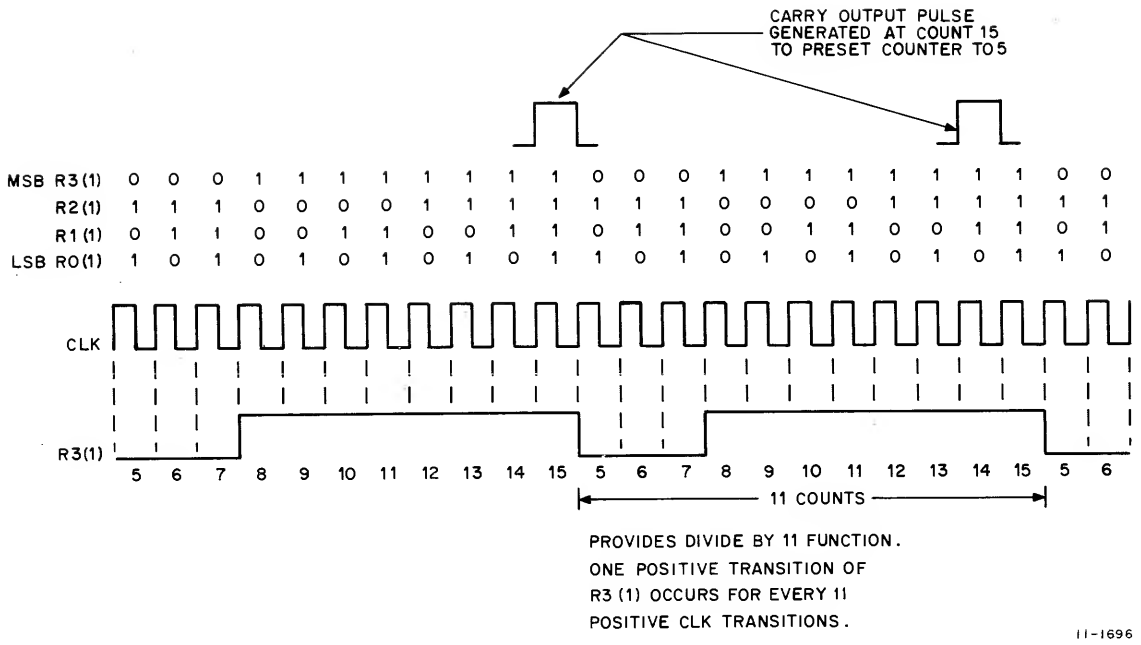


Figure 4-9 Divide by 11 Function of 74161 Counter E03

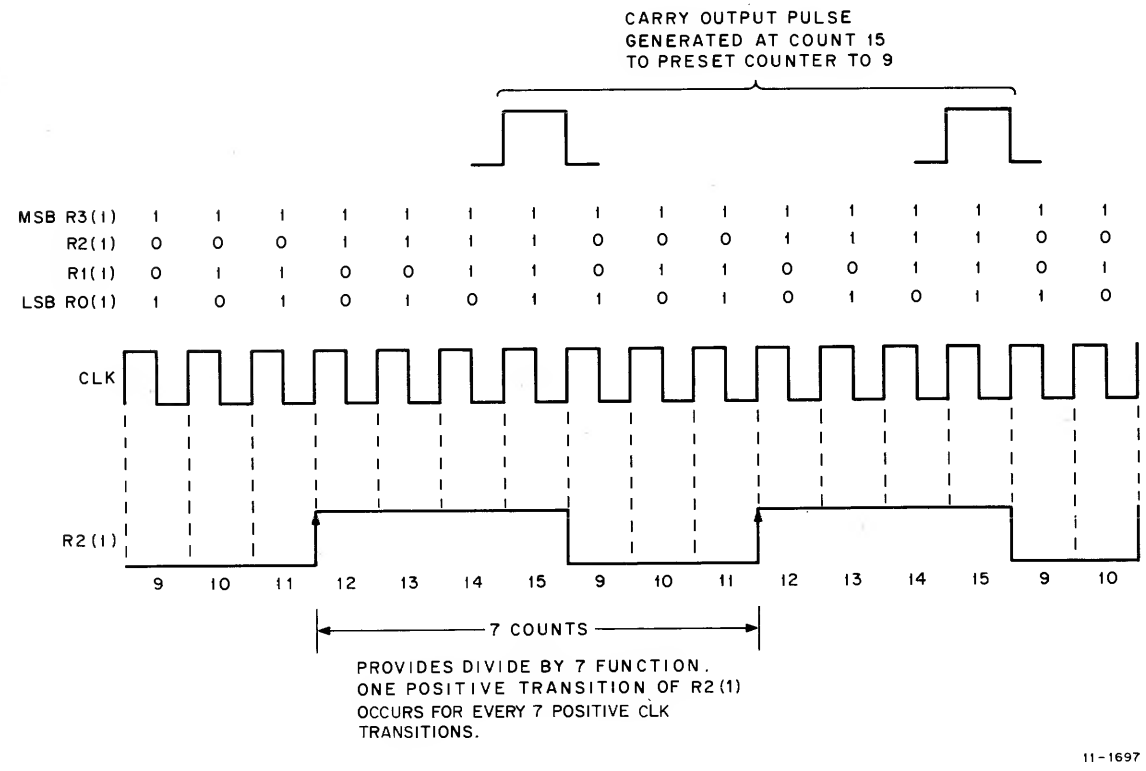


Figure 4-10 Divide by 7 Function of 74161 Counter E08

4.3.3 Count Down Sequence

This discussion traces the oscillator output through the clock logic print (D-CS-4540-0-1, sheet 2) to show how and where the 16 Baud rates are generated. Additional aids include Figure 4-11 which is a simplified block diagram of the clock, and Table 4-4 which lists the clock output signals and sources.

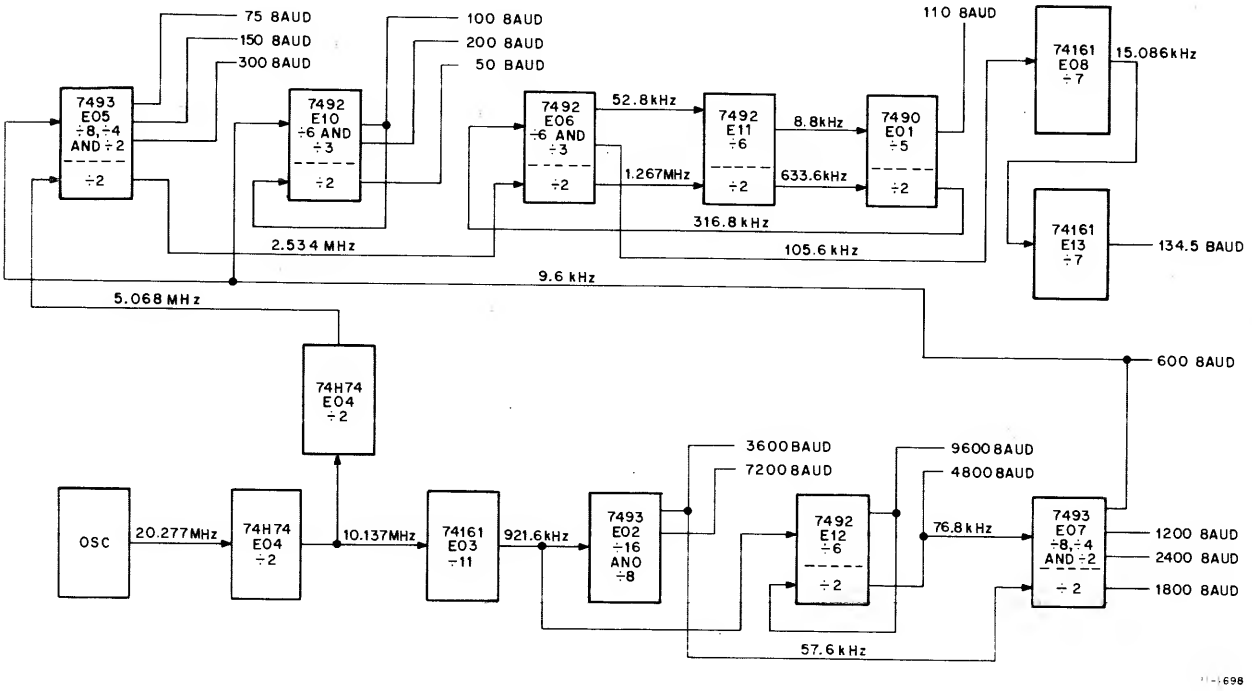


Figure 4-11 Simplified Block Diagram of Clock

Table 4-4
Clock Output Signals

Signal Source		Baud	Frequency (Hz)	Period (μs)
Pin No.	Device			
B1	E12 pin 08	9600	153,600	6.5
C1	E02 pin 08	7200	115,200	8.8
N1	E12 pin 12	4800	76,800	13.0
A1	E02 pin 11	3600	57,600	17.4
D1	E07 pin 09	2400	38,400	26.0
U2	E07 pin 12	1800	28,800	34.7
J1	E07 pin 08	1200	19,200	52.1
S1	E07 pin 11	600	9,600	104
L1	E05 pin 09	300	4,800	208
R1	E10 pin 09	200	3,200	313
K1	E05 pin 08	150	2,400	417
V2	E13 pin 12	134.5	2,152	465
H1	E01 pin 11	110	1,760	568
T2	E10 pin 08	100	1,600	625
F1	E05 pin 11	75	1,250	833
P1	E10 pin 12	50	800	1250

NOTE: Frequency in Hz is 16 times Baud.

The crystal controlled oscillator starts operating when +5 V power is applied. Once started, it is free running and supplies a 20.277 MHz signal to pin 01 of gate E09. This gate inverts the signal and sends it to the clock input (pin 03) of flip-flop E04. This clock input is divided by 2 and appears at the complementary flip-flop outputs as a 10.138 MHz signal. The (1) H output (pin 05) of the flip-flop is sent to the CLK input of counter E03. This type 74161 counter functions as a divide by 11 counter. Its output signal, which is 921.6 kHz, is taken from the R3 (1) output and sent to the CLK 0 input of counter E02 and the CLK BC input of counter E12.

Counter E02 is a type 7493 that functions as a 4-bit ripple-through counter. Output R2 (1) represents a divide by 8 function that produces a 115.2 kHz signal. This is the 7200 Baud signal and is brought out to module pin C1. Output R3 (1) represents a divide by 16 function that produces a 57.6 kHz signal. This is the 3600 Baud signal and is brought out to module pin A1.

Counter E12 is a type 7492 that operates as a divide by 6 counter and a divide by 2 counter. The CLK BC input (921.6 kHz) is divided by 6 to produce a 153.6 kHz signal at output R3 (1). This is the 9600 Baud signal and is brought out to module pin B1. Output R3 (1) is also fed back to the CLK 0 input. It is divided by 2 to produce a 76.8 kHz signal at output R0 (1). This is the 4800 Baud signal and it is brought out to module pin N1.

The 3600 Baud output of counter E02 is sent to the CLK 0 input of counter E07; and the 4800 Baud output of counter E12 is sent to the CLK BC input of counter E07. Counter E07 is a type 7493 that functions as a 3-bit ripple-through counter and a modulo 2 counter. Outputs R3 (1), R2 (1), and R1 (1) are the outputs of the 3-bit ripple-through counter associated with the CLK BC input (4800 Baud or 76.8 kHz). These outputs represent the following functions:

Divide by 8 at R3 (1) generates 600 Baud (9.6 kHz)
Divide by 4 at R2 (1) generates 1200 Baud (19.2 kHz)
Divide by 2 at R1 (1) generates 2400 Baud (38.4 kHz)

These signals are brought out to the following module pins: pin S1 for 600 Baud, pin J1 for 1200 Baud, and pin D1 for 2400 Baud.

Output R0 (1) of counter E07 represents a divide by 2 function for the CLK 0 input. This produces the 1800 Baud (28.8 kHz) signal that is brought out to module pin U2.

At this point in the discussion, refer back to the first divide by 2 function performed by flip-flop E04. The (0) H output (pin 06) of this flip-flop is sent to the clock input (pin 11) of the other E04 flip-flop. Another divide by 2 function is performed by this flip-flop and its (0) L output signal, which is 5.068 MHz, is sent to the CLK 0 input of counter E05. The CLK BC input of E05 is supplied with the 600 Baud (9.6 kHz) signal from counter E07.

Counter E05 is a type 7493 that functions as a 3-bit ripple-through counter and a modulo 2 counter. Outputs R3 (1), R2 (1), and R1 (1) are the outputs of the 3-bit ripple-through counter associated with the CLK BC input (600 Baud or 9.6 kHz). These outputs represent the following functions:

Divide by 8 at R3 (1) generates 75 Baud (1.2 kHz)
Divide by 4 at R2 (1) generates 150 Baud (2.4 kHz)
Divide by 2 at R1 (1) generates 300 Baud (4.8 kHz)

These signals are brought out to the following module pins: pin F1 for 75 Baud, pin K1 for 150 Baud, and pin L1 for 300 Baud.

Output R0 (1) of counter E05 represents a divide by 2 function for the CLK 0 input. This produces the 2.534 MHz signal that is sent to the CLK 0 input of counter E06.

The 600 Baud (9.6 kHz) signal from counter E07 is also sent to the CLK BC input of counter E10. This type 7492 counter operates as a divide by 6 counter and a divide by 2 counter. The divide by 6 counter is associated with the CLK BC input and output R3 (1), R2 (1), and R1 (1). Output R3 (1) represents a divide by 6 function that produces the 100 Baud (1.6 kHz) signal that is brought out to module pin T2. Output R2 (1) represents a divide by 3 function that produces the 200 Baud (3.2 kHz) signal that is brought out to module pin R1. Output R3 (1) is also fed back to the CLK 0 input. It is divided by 2 to produce the 50 Baud (800 Hz) signal at output R0 (1) that is brought out to module pin P1.

Counter E06 is a type 7492 that operates as a divide by 6 counter and a divide by 2 counter. Input CLK 0 is fed by the 2.534 MHz signal from output R0 (1) of counter E05. Input CLK BC is fed by the 316.8 kHz signal from output R0 (1) of counter E01. The divide by 6 counter is associated with the CLK BC input and produces a divide by 6 function (52.8 kHz) at output R3 (1) and a divide by 3 function (105.6 kHz) at output R2 (1). The divide by 2 counter is associated with the CLK 0 input and produces a 1.267 MHz signal at output R0 (1). The R3 (1) output (52.8 kHz) is sent to the CLK BC input of counter E11; the R2 (1) output is sent to the CLK input of counter E08; and the R0 (1) output is sent to the CLK 0 input of counter E11.

Counter E11 is a type 7492 that operates the same as counter 06. It provides a divide by 6 function (8.8 kHz) at output R3 (1) and a divide by 2 function (633.6 kHz) at output R0 (1). The R3 (1) output is sent to the CLK B0 input of counter E01 and the R01 (1) output is sent to the CLK 0 input of counter E01.

Counter E01 is a type 7490 that operates as a divide by 5 counter and a divide by 2 counter. The CLK BC input (8.8 kHz) is divided by 5 and appears at output R3 (1) as the 110 Baud (1.76 kHz) signal and is brought out to module pin H1. The CLK 0 input (633.6 kHz) is divided by 2 and appears at output R0 (1) as a 316.8 kHz signal that is sent to the CLK BC input of counter E06.

The R2 (1) output (105.6 kHz) of counter E06 is sent to the CLK input of counter E08. This type 74161 counter functions as a divide by 7 counter. Its output signal, which is 15.086 kHz, is taken from the R2 (1) output and sent to the CLK input of counter E13. Counter E13 is also a type 74161 that functions as a divide by 7 counter. Its output signal is taken from output R2 (1). It is the 134.5 Baud (2.155 kHz) signal and is brought out to module pin V2.

The outputs of the clock module are sent to the M7288 Line Parameter Control Module where they are switched to the appropriate UART receivers and transmitters on the M7280 Multiple UART cards.

The 5.068 MHz signal from flip-flop E4 pin 9 is sent to the M7279 FIFO Buffer Module. The 2.534 MHz signal from the R0 (1) output of counter E5 is sent to the M7289 System Control and Receiver Scanner Module.

4.4 LINE PARAMETER CONTROL MODULE M7288

4.4.1 Introduction

The M7288 Line Parameter Control Module contains logic that performs the following functions for the line selected by the System Control Register (SCR):

a. Selects transmitter speed
b. Selects receiver speed
c. Selects half duplex or full duplex operations
d. Enables auto-echo feature

Signals for controlling these functions come from the outputs of the Line Parameter Register (LPR) and the control strobe generation logic on the Current Address and Address Selector Module M7277. The function signals are sent from the M7288 Line Parameter Control Module to the appropriate UART inputs. Signals for controlling other UART functions are sent directly from the LPR to the UARTs. These other functions include character length, number of stop bits, parity enable, and odd or even parity.

The physical layout of the M7288 module corresponds with the nine sheets of logic (drawing D-CS-M7288-0-1, sheets 3 – 11) as shown in Figure 4-12. Sheet 3 contains the buffers for incoming signals. Transmission speed selection logic is shown in the following sheets:

a. Sheet 4 for lines 00 – 03
b. Sheet 6 for lines 04 – 07
c. Sheet 8 for lines 08 – 11
d. Sheet 10 for lines 12 – 15

Logic for receiver speed selection, half duplex or full duplex selection, and auto-echo enable is shown in the following sheets:

a. Sheet 5 for lines 00 – 03
b. Sheet 7 for lines 04 – 07
c. Sheet 9 for lines 08 – 11
d. Sheet 11 for lines 12 – 15

4.4.2 Signal Buffering

Nearly all the signals sent to the M7288 module are buffered before being used. Buffering is necessary to provide adequate drive for the multiple use of these signals.

All the buffering is provided by 11 type 7437 2-input NAND buffers that are shown in print D-CS-M7288-0-1, sheet 3. Each of the 16 selectable transmitter/receiver speeds is buffered twice. This requires 32 buffers or 8 type 7437 packages (E66, E67, E69, E70, E72, E73, E74, and E75). For example, signal 50 BAUD H on module pin FP1 is buffered by E69 to provide TOP BUFF 50 BAUD H and by E66 to provide BOT BUFF 50 BAUD H. The TOP BUFF signals are inputs to the top row of 16 type 74150 multiplexers and the BOT BUFF signals are inputs to the bottom row of 16 type 74150 multiplexers (Figure 4-12).

The speed signals are inverted by the buffers; however, this fact is not revealed in the signal designation. The level designation for the buffer input and output signals are both represented as highs (H). This is done to obtain consistency in showing the interconnections between the buffers and other devices. This should not cause any confusion because the speed signals are clock signals in which edge transitions are more significant than logic levels.

Bits LPR 06 L – LPR 15 L from the LPR are also buffered. Ten buffers or two and one half 7437 packages are used (E65, E68, and 1/2 of E71). The remaining two gates in package E71 are used to buffer INIT A H from the M7288 module to produce BUFF INIT A L and BUFF INIT B L. These two buffered signals are used to provide adequate drive for the multiple use of the initialize (INIT) signal.

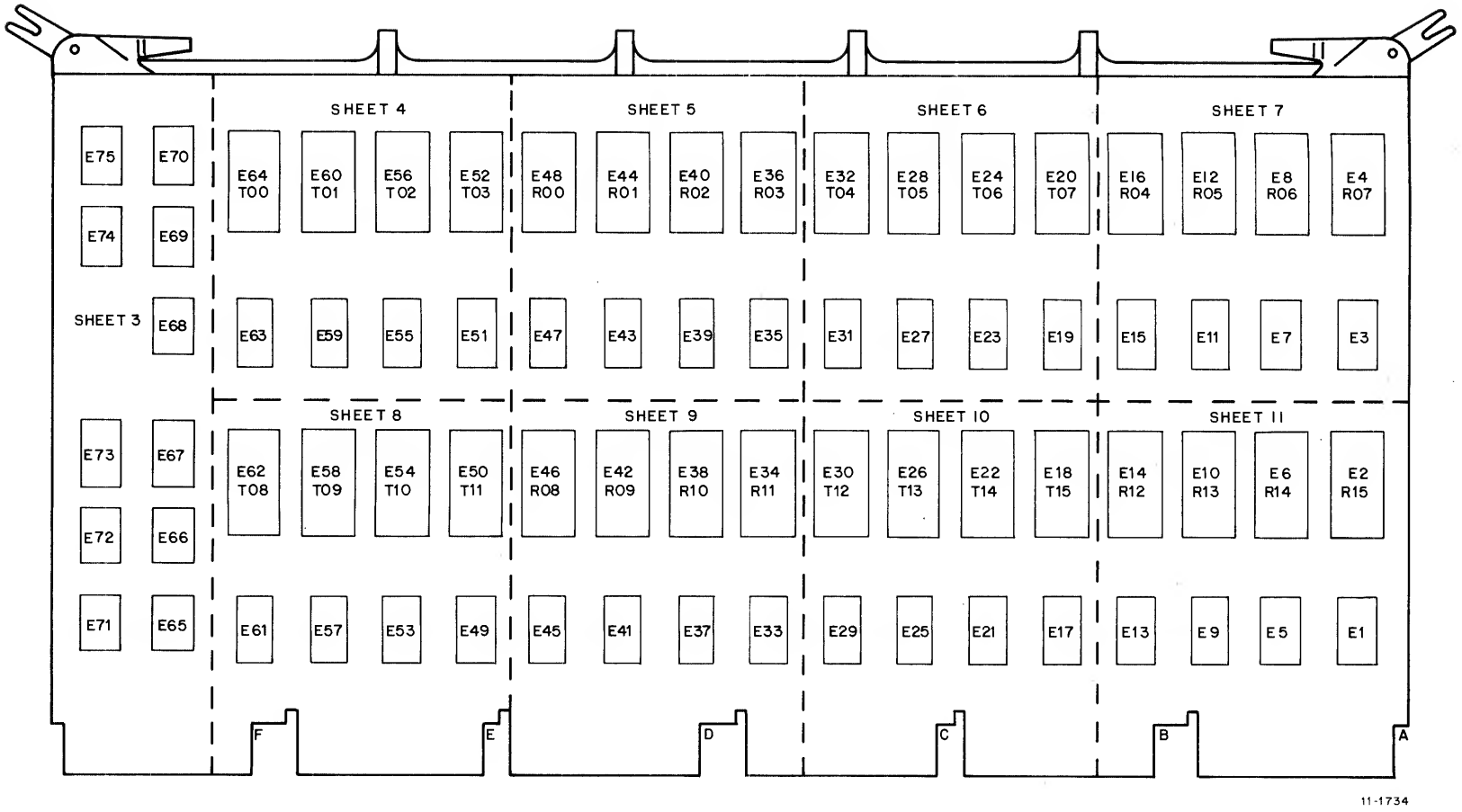


Figure 4-12 Component Layout of M7288 Module

4.4.3 Overall Operation

Associated with each of the 16 lines is a transmitter clock multiplexer and a receiver clock multiplexer (Figure 4-13). Each multiplexer is a type 74150 that selects 1 of 16 data inputs. The 16 data inputs are the buffered speed signals that are sent to all 32 multiplexers. Input selection is determined by the four multiplexer select lines that select on an equivalent number basis; for example, if the select lines represent decimal 5, input D05 is selected and enabled to the output. The select lines are controlled by signals from the LPR that specify transmitter and receiver speed. For transmitter speed selection, signals BUFF LPR 10 H – BUFF LPR 13 H are used; and for receiver speed selection, signals BUFF LPR 06 H – BUF LPR 09 H are used. These buffered LPR signals are sent to 4-bit flip-flop registers associated with each multiplexer. For the transmitter multiplexers, the registers are type 74175 quad D-type flip-flops. For the receiver multiplexers, the registers are type 74174 hex D-type flip-flops. The two extra bits are used for the auto-echo enable signal and the half duplex, full duplex selection signal.

The flip-flop outputs are enabled to the multiplexer select inputs when the flip-flops are clocked. Sixteen clock signals are used (one for each line). They are generated on the M7277 module as a function of the line selected by the System Control Register and are called CONTROL STROBE LINE 00 H, 01 H, etc. The 74175 package associated with the transmitter multiplexer for a particular line, and the 74174 package associated with the receiver multiplexer for the same line, use a common clock signal. Thus, the desired transmitter and receiver speeds are sent to the appropriate UART when the selected clock (Control Strobe) signal is enabled.

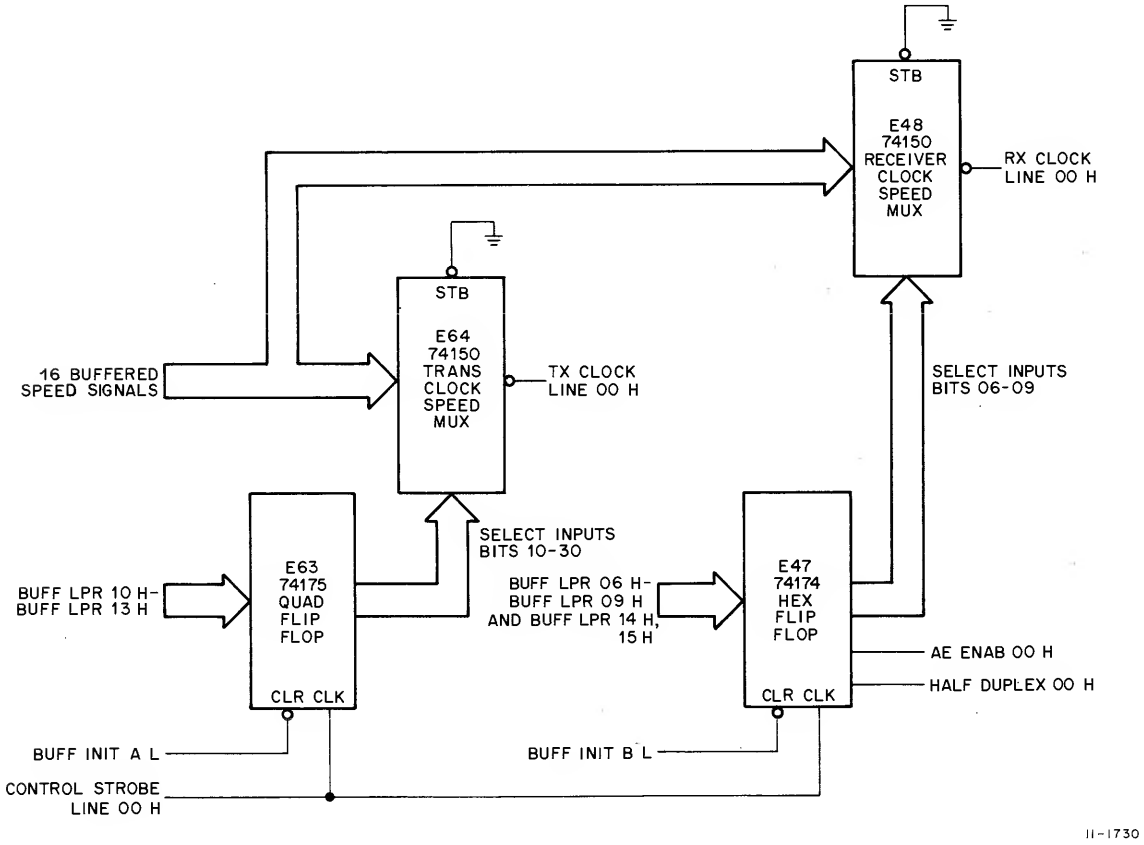


Figure 4-13 Block Diagram of Transmitter and Receiver Speed Selection for Line 00

As previously stated, one bit of the 74174 hex flip-flop package is used to enable the auto-echo feature. The selection signal for this function is bit 15 from the LPR (BUFF LPR 15 H). Also, one bit is used to select half duplex or full duplex operation. The selection signal for this function is buffered bit 14 from the LPR (BUFF LPR 14 H). The auto-echo enable and half/full duplex function signals are taken from the output of the 74174 and sent to logic on the M7289 module.

4.4.4 Transmitter Speed Selection

This discussion covers selection of a particular transmitter speed for a desired line. Only one example is discussed because the process is the same for all 16 lines. The example shows the selection of 110 Baud for the transmitter used on line 00 (Figure 4-14).

E64 is a type 74150 multiplexer that selects 1 of 16 data inputs. These inputs are the buffered speed signals from drawing D-CS-M7288-0-1, sheet 3 (TOP BUFF signals only). Inputs D01 – D13 are speed signals that originate on the M4540 Clock Module. Input D00 is the 0 Baud signal and inputs D14 and D15 are external inputs. The user can connect an external clock to these inputs, D14, or D15. Signals of 100, 3600, and 7200 Baud from the clock module can be connected to the external inputs or an M401 or M405 Clock Module may be installed in slot E09 or slot B06. These signals are available on the clock module but are not program selectable except through the external inputs.

First set SCR bits 0 – 3 to all 0s to select line 00. Assume that the operation starts with flip-flop register E63 cleared (all outputs are 0). This selects 0 Baud which turns off the transmitted clock for line 00. Now, it is desired to select 110 Baud for the transmitter on line 00. The program selects the states of the LPR bits to request 110 Baud as follows:

LPR Bit	13	12	11	10
State	0	0	1	1

These bits are written into the LPR, which is a flip-flop register with complementary outputs. Bits 10 – 13 are taken from the 0-output of the flip-flop.

These signals (LPR 10 L – LPR 13 L) are sent from the M7278 module to the M7288 module and inverted by the type 7437 NAND buffers to produce BUFF LPR 10 H – BUFF LPR 13 H (drawing D-CS-M7288-0-1, sheet 3). These buffered signals are sent to the D inputs of type 74175 quad flip-flop E63. The 1-outputs of this device are connected to the select inputs (S0 – S3) of type 74150 multiplexer E64. When E63 is clocked, the select input states are the same as those selected by the program to pick the 110 Baud signal.

The clock signal for E63 is CONTROL STROBE LINE 00 H from the Current Address and Address Selector Module M7277. Normally, this signal is low. When the System Control Register selects line 00 and the program loads the LPR, the trailing edge of the LOAD LPR H signal triggers 300 ns one-shot E61 on Module 7277 and causes CONTROL STROBE LINE 00 H to go high. This positive transition clocks E63 and its 1-outputs are sent to the select inputs of E64. These inputs represent decimal 3 which selects input D03 (TOP BUFF 110 BAUD H). This signal is enabled to the output of E64 in complemented form as TX CLOCK LINE 00 L which is sent to the transmitter clock input of the UART for line 00.

4.4.5 Receiver Speed Selection

Receiver speed selection is very similar to transmitter speed selection. This discussion shows the selection of 600 Baud for the receiver used on line 03 (Figure 4-15). The discussion is not detailed because of the similarity to the transmitter speed selection covered in Paragraph 4.4.4.

Multiplexer E36 is used for line 03 and its associated flip-flop register (E35) is a type 74174 that contains six D type flip-flops.

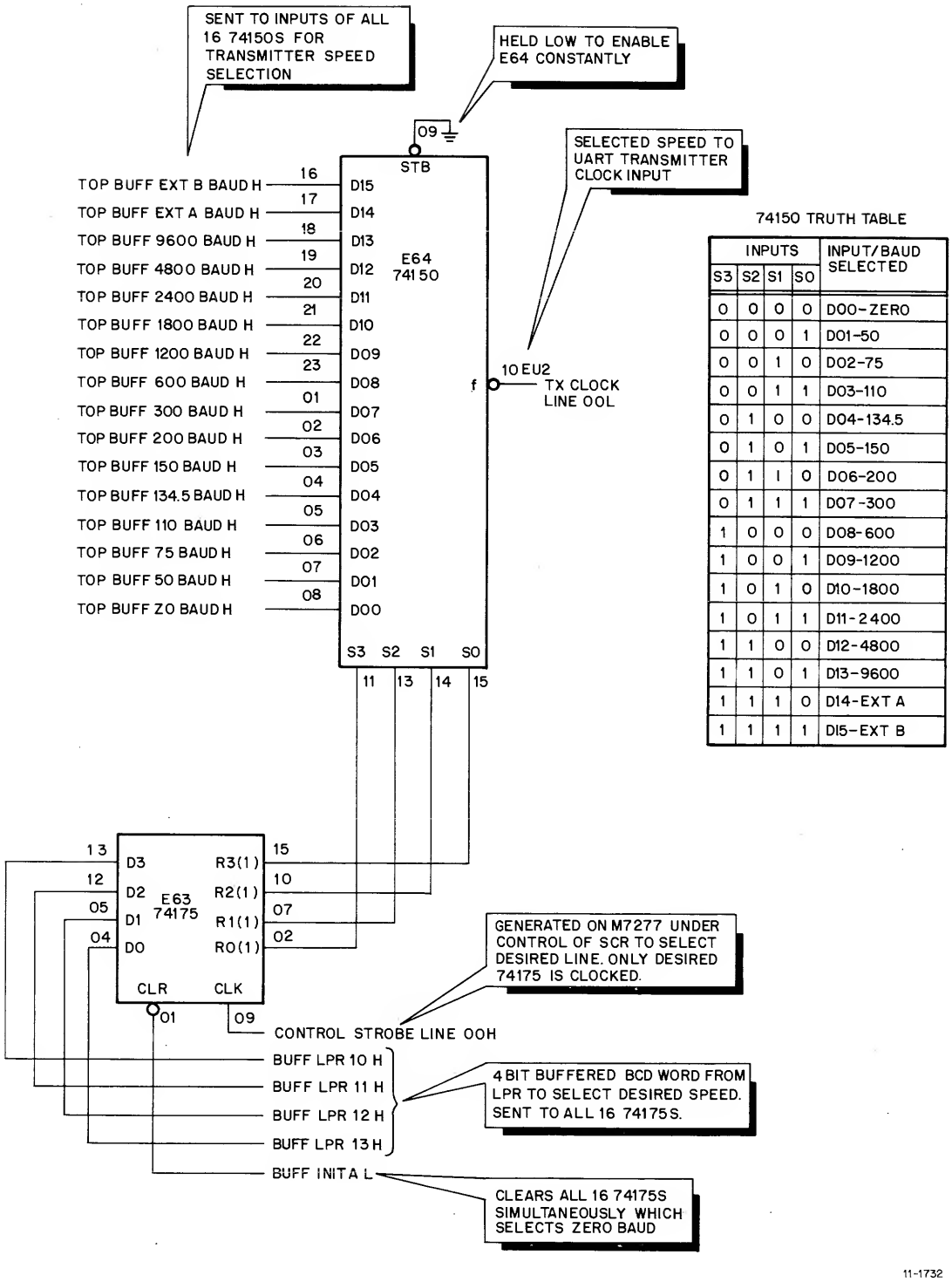


Figure 4-14 Typical Transmitter Speed Selection Circuit

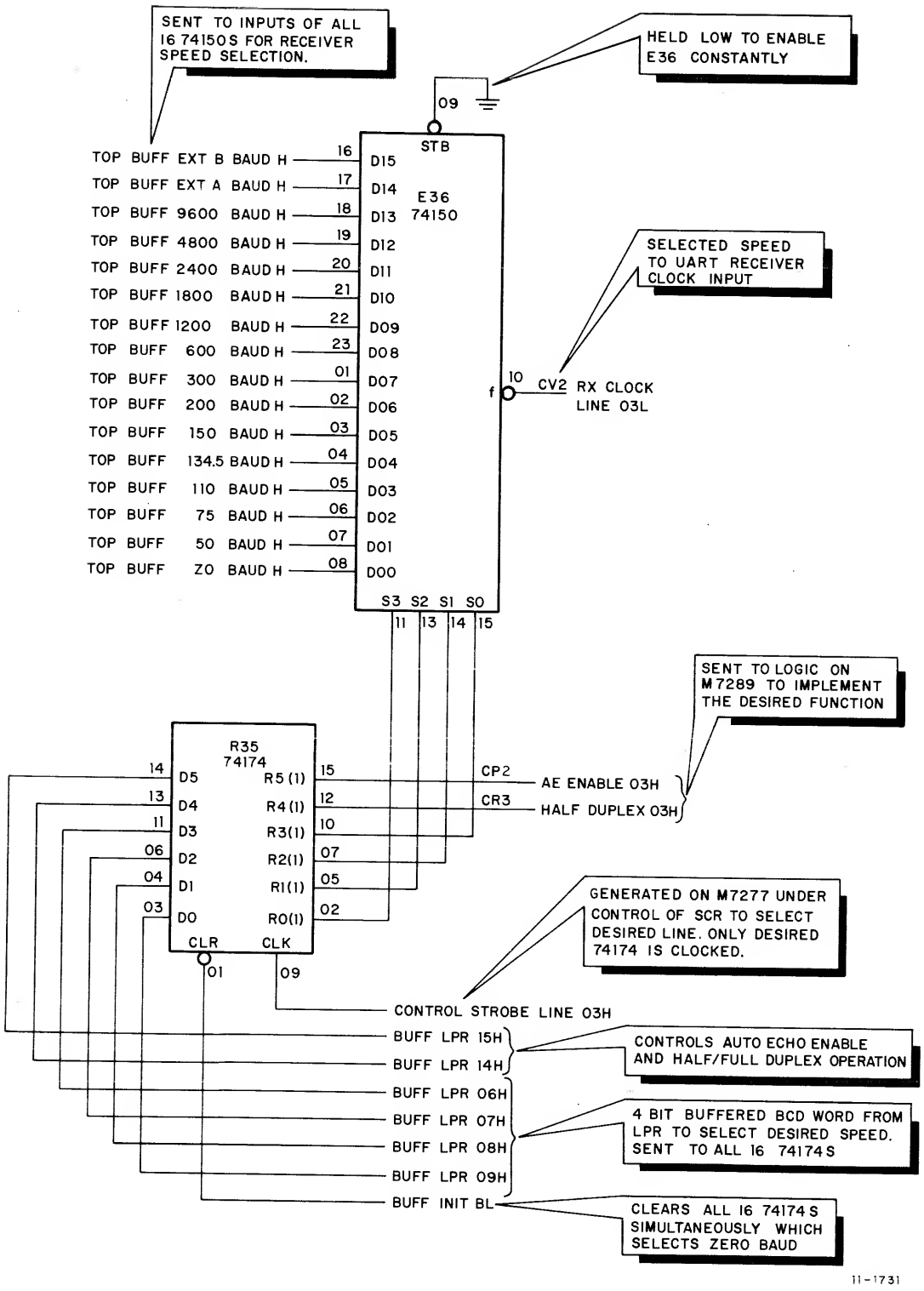


Figure 4-15 Typical Receiver Speed Selection Circuit

To select 600 Baud, the program first sets SCR bits 03 – 00 to 0011 to select line 03 and then writes into the LPR as follows:

LPR Bit	09	08	07	06
State	1	0	0	0

These bits are taken from the 0 outputs of the LPR and inverted by the M7288 buffers. This produces signals BUFF LPR 06 H – BUFF LPR 09 H which are sent to E35 to control the select inputs of E36. When E35 is clocked, the select input states represent decimal 8 which selects input D08 (TOP BUFF 600 BAUD H).

The clock signal for E35 is CONTROL STROBE LINE 03 H which is generated on module M7277 at the conclusion of the instruction that loaded the LPR. The output of E36 is RX CLOCK LINE 03 L which is sent to the receiver clock input of the UART for line 03.

4.4.6 Auto-Echo Enable and Half/Full Duplex Control Signals

The auto-echo enable and half/full duplex control signals for each line are taken from the type 74174 flip-flop register associated with the receiver speed selection logic. LPR bit 14 is the half/full duplex control signal and LPR bit 15 controls the auto-echo enable bit. If the program sets LPR bit 14, half duplex operation is selected. If the program sets LPR bit 15, the auto-echo feature is enabled.

These signals are taken from the 0 outputs of the LPR and inverted by the M7288 buffers. This produces signals BUFF LPR 14 H and BUFF LPR 15 H which are sent to all 16 type 74174 hex flip-flop registers.

For a specific example, assume that it is desired to select full duplex operation and enable the auto-echo feature for line 03. First, the program loads the SCR to select line 03. Next, the LPR is loaded to select full duplex (LPR bit 14 is cleared) and auto-enable (LPR bit 15 is set). The complements of bits 14 and 15 are taken from the LPR, inverted by the M7288 buffers, and applied to flip-flop register E35. BUFF LPR 14 H, which is low, is sent to E35 input D4. BUFF LPR 15 H, which is high, is sent to E35 input D5 (drawing D-CS-M7288-0-1, sheet 5). At the end of the LPR load operation, CONTROL STROBE LINE 03 H is generated to clock E35. Signal HALF DUPLEX 03 H is low and signal AE ENAB 03 H is high. These signals are sent to logic on the M7289 module to implement the requested functions; that is, to operate line 03 in full duplex and to enable the auto-echo feature on line 03.

4.5 TRANSMITTER SCANNER

4.5.1 Introduction

The transmitter scanner logic is located on the M7277 Current Address and Address Selector Module (drawing D-CS-M7277-0-1, sheet 4). This discussion deals with the detailed operation of the scanner.

4.5.2 Functional Description

Part of the process used to initiate transmission requires that the bit in the Buffer Active Register (BAR) associated with the selected line be set. This bit is ANDed with the Transmitter Buffer Empty (TBMT) flag from the associated UART (Figure 4-16). This flag is set when the UART data bit Holding Register can be loaded with a message character. The TBMT flag and BAR bit are ANDed for all 16 lines (AND gate E70 shown for line 15). The AND gate outputs are sent to the inputs of E45 which is a type 74150 16-to-1 multiplexer. The E45 select inputs are controlled by the outputs of counter E49 which is a type 74193 synchronous 4-bit binary counter. It is connected to count up from decimal 0 to 15. If no line has its BAR bit set, the scanner continually scans the lines sequentially. When it is desired to initiate transmission on a particular line, its BAR bit is set by the program after first having loaded a current address and byte count for that line. The UART associated with this line sets its TBMT flag when it is ready to accept a character for transmission.

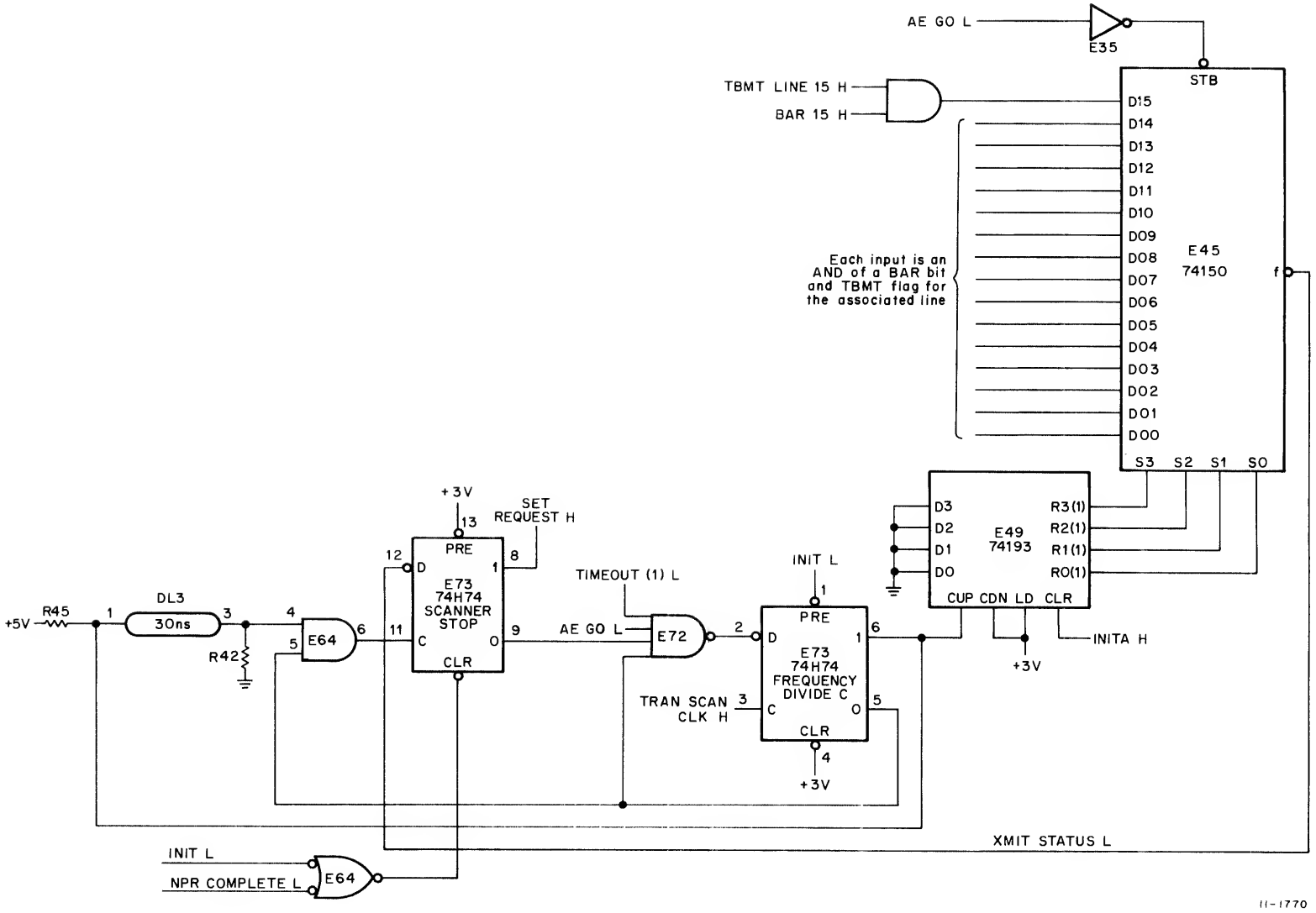


Figure 4-16 Transmitter Scanner Logic

The ANDing of BAR XX H and TBMT LINE XX H puts a high on input XX of the multiplexer. When line XX is scanned, a low signal is generated at the multiplexer output. This signal is sent to the D-input of the SCANNER STOP flip-flop which is a redefined flip-flop. When the SCANNER STOP flip-flop sets, SET REQUEST H goes high. This signal is sent to the M796 Unibus Master Control Module to initiate the action that allows the DH11 to become bus master and take the message to be transmitted from memory. A low signal from the SCANNER STOP flip-flop 0-output disqualifies gate E72 and puts a high on the D input of the FREQ DIV C flip-flop. This redefined flip-flop is reset and it stays in this state as long as E72 is disabled. This eliminates the source of clock pulses for the E49 counter. When a character has been loaded into the UART from memory, NPR COMPLETE L is asserted which clears the SCANNER STOP flip-flop and allows the scanner to restart. It scans until another line is found that has its BAR bit set. When the transmission on a line is complete, the BAR bit is cleared. NPR COMPLETE L occurs once per character. The BAR bit is cleared once per message.

4.5.3 Logic Description

To understand the basic operation of the scanner, assume that no transmitters are activated and a previous transmission has just been completed. No BAR bits are set which means that bits BAR 00 H – BAR 15 H are all low. As a result, the outputs of all 7408 AND gates are low (Figure 4-16). These 16 low signals are sent to the inputs of E45 which is a type 74150 16-to-1 multiplexer. Input selection is determined by the four multiplexer select lines (S0 – S3) which constitute a 4-bit BCD word. Selection is made on an equivalent number basis; for example, if the select lines represent decimal 6, input D06 is selected and enabled to the output. The multiplexer is enabled by a low signal to the strobe (STB) input. This signal is AE GO L and is inverted by E35 before being applied to the strobe. Normally, AE GO L is high, and after inversion, supplies the required low strobe signal. When the auto-echo feature is enabled, AE GO L is low and the multiplexer is disabled (output is high).

The multiplexer select inputs (S0 – S3) are controlled by the outputs of counter E49. It is a type 74193 synchronous 4-bit up/down counter. In this application, it is connected to count up only by sending the clock signal to the count up (CUP) input while the count down (CDN) input is held high. The data inputs (D0 – D4) are not used and the load input (LD) is disabled by connecting it to +3 V. The counter cannot be preset so it counts up from decimal 0 – 15, overflows, and continues up counting and overflowing as long as clock pulses (positive transitions) are supplied.

Under the assumed condition that no transmitter is activated, all inputs to the multiplexer are low. As the counter is incremented and each low input is scanned, the multiplexer output (f) remains high. Note that the output is the complement of the selected input. This signal is sent to the D input of the redefined SCANNER STOP flip-flop. This flip-flop controls the scanner operation by allowing or disallowing clock pulses to be sent from the FREQUENCY DIVIDE C flip-flop 1-output to the counter clock input. When the multiplexer output is low, the scanner stops; when the multiplexer output is high, the scanner continues to increment.

Assume that the SCANNER STOP flip-flop has been cleared by NPR COMPLETE L. In this state, the 1-output (SET REQUEST H) of the SCANNER STOP flip-flop is low, which means that no action is taken by the M796 module to make the DH11 bus master. The 0-output of the SCANNER STOP flip-flop is high and is sent to E72 which is a 4-input NAND gate. The other inputs to E72 are: the 0-output of the FREQUENCY DIVIDE C flip-flop, TIMEOUT (1) L, and AE GO L. The last two mentioned signals are normally high. When either signal is low, the scanner stops. The operation of TIMEOUT (1) L and AE GO L are described in subsequent paragraphs. For now, assume that they are both high.

The FREQUENCY DIVIDE C flip-flop is connected to operate in the toggle mode. The 0-output of the flip-flop is fed back to the D input via gate E72 so that the flip-flop changes state at each positive edge of the clock signal (TRAN SCAN CLK H = 1.2 MHz). This produces pulse trains at the flip-flop 1 and 0 outputs that have a frequency of 600 kHz.

The 1-output of the FREQUENCY DIVIDE C flip-flop is sent to the count up (CUP) input of counter E49. These pulses increment the counter (transmitter scanner). The 1-output is also sent to pin 4 of 2-input AND gate E64 via the 30 ns delay line DL3. The 0-output of the FREQUENCY DIVIDE C flip-flop is sent to gate E72 and to the other input (pin 5) of gate E64. The output of E64 is a positive pulse of approximately 30 ns that starts on the negative transition of the FREQUENCY DIVIDE C flip-flop output. This sequence is illustrated in the timing diagram shown in Figure 4-17. The output of E64 is the clock signal for the SCANNER STOP flip-flop.

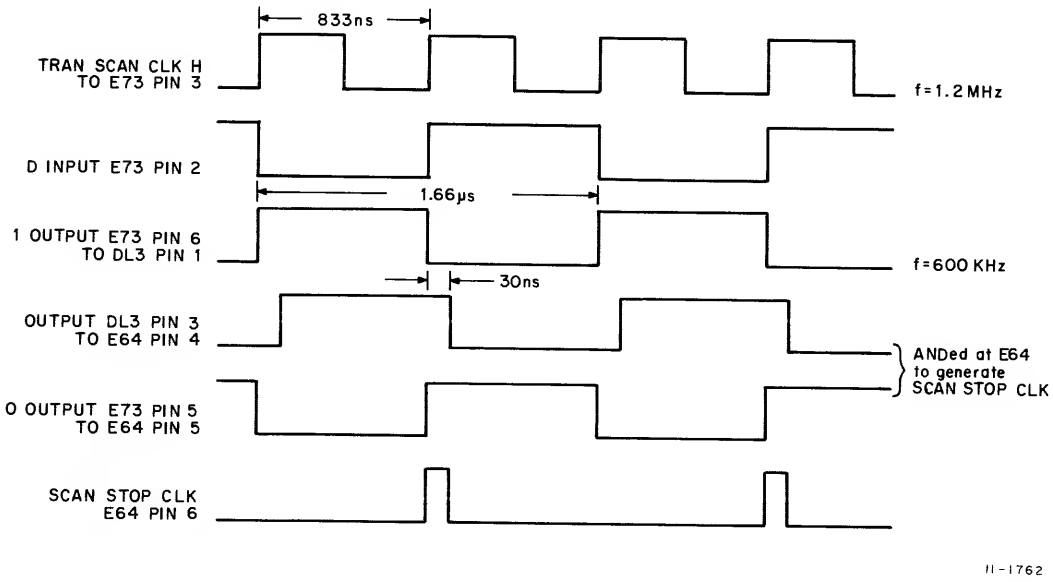


Figure 4-17 Timing Diagram for Generation of Scanner Stop Flip-Flop Clock Signal

To summarize, as long as the multiplexer output is high, the SCANNER STOP flip-flop is cleared and the FREQUENCY DIVIDE C flip-flop continues to toggle. Counter E49 is incrementing and the scanner is operating.

Assume now that transmission is desired on line 12. BAR 12 H is set by the program and UART number 12 asserts TBMT LINE 12 H. This occurs whenever the transmitter holding buffer in UART number 12 is empty. Input D12 of multiplexer E45 is now high. When counter E49 reaches the count of 12, input D12 is enabled to the output of E45 which now becomes low. This puts a low on the D input of the SCANNER STOP flip-flop. On the next positive edge of the SCANNER STOP clock signal, the flip-flop is set. Its 1-output (SET REQUEST H) is high which initiates action in the M796 module to make the DH11 bus master. The SCANNER STOP flip-flop 0-output is low which disables gate E72. This puts a high on the D input of the FREQUENCY DIVIDE C flip-flop. On the next positive edge of the clock signal (TRAN SCAN CLK H), the flip-flop is reset. The FREQUENCY DIVIDE C flip-flop remains in the reset condition which inhibits the clock signal to counter E49 and inhibits the generation of clock signals to the SCANNER STOP flip-flop which remains in the set condition. The scanner stops at input D12 until the loading of the character to be transmitted is complete, at which time NPR COMPLETE L clears the SCANNER STOP flip-flop and allows the scanner to resume operation.

The scanner can be stopped when TIMEOUT (1) L to gate E72 is asserted. This occurs when the current address logic tries to address non-existent memory. It is also stopped when AE GO L is asserted. This occurs when the auto-echo feature is enabled.

4.6 CURRENT ADDRESS REGISTER AND CONTROL LOGIC

4.6.1 Introduction

The Current Address Register (CAR) and associated control logic are located on the M7277 Current Address and Address Selector Module (drawing D-CS-M7277-0-1, sheets 5 and 6). This discussion deals with the detailed operation of this logic and is divided into three parts. The first part describes how the CAR is loaded, incremented, and read. The second part describes the logic that controls the operation of the CAR. The third part describes the byte control logic which is associated with the CAR.

4.6.2 Current Address Register

4.6.2.1 Functional Description – In the transmit mode, the program loads the Current Address Register (CAR) with the memory address of the first character of the message to be transmitted on the selected line. The program also loads a byte count and sets a BAR bit. Using an NPR, the DH11 becomes Unibus master and places the CAR address on the Unibus address lines. A DATI is performed which brings the desired character (as a byte) from the memory to the DH11. During this transaction, the CAR is incremented by 1 so that it contains the address of the next character to be retrieved from memory during the next DATI transaction. This process continues until the last character is transferred. The CAR can be read by the program.

4.6.2.2 Components – The CAR consists of the following major components (drawing D-CS-M7277-0-1, sheets 5 and 6):

a. Five type 7489 64-bit read/write memories (E4, E11, E18, E25, and E31), with common address lines and enabling inputs to form a 16-word by 18-bit memory.

b. Five type 74193 synchronous 4-bit counters (E5, E12, E19, E26, and E32), cascaded to provide an 18-bit counter.

c. Five type 74157 quad 2-line to 1-line multiplexer (E6, E13, E20, E27 and E33) with a common select signal to provide an 18-bit multiplexer.

A multiplexer, counter, and memory are interconnected to accommodate 4 bits of the CAR. All but 2 bits of one group of devices (E31, E32, and E33) are used to handle the 18-bit capacity of the CAR. A typical 4-bit section of the CAR is shown in Figure 4-18.

E4 is a type 7489 64-bit read/write semiconductor (TTL) memory organized in 16 4-bit words. The 16 words are addressed by the 4-bit binary word sent to address lines A0 – A3. The 4-bit data word is sent to inputs D0 – D3. In this application, the enabling input (ENB) is permanently held low; therefore, for a selected word, a write operation is performed when the write (WR) input is low and a read operation is performed when the write (WR) input is high. A write operation places the input data into the selected word. In a read operation, the complement of the information that has been written into the selected word is non-destructively read out at the four outputs.

E5 is a type 74193 synchronous 4-bit counter. The data inputs are D0 – D3 and the corresponding outputs are R0 (1) – R3 (1). It is operated in the count up mode by holding the count down (CDN) input permanently high while applying clock pulses to the count up (CUP) input. The positive (trailing) edge of the clock pulse increments the counter. The outputs can be preset to any state by entering the desired data at the data inputs while the load (LD) input is low. Counters are cascaded in the CAR by connecting the carry (CRY) and borrow (BRW) outputs to the count up (CUP) and count down (CDN) inputs, respectively, of the succeeding counter.

E6 is a type 74157 quad 2-line to 1-line multiplexer. The four outputs (f0 – f3) represent either the A word input or the B word input as selected by the state of the select (S0) input. The strobe (STB) input is permanently held low, which enables the multiplexer; with S0 low, the A word is selected and with S0 high, the B word is selected.

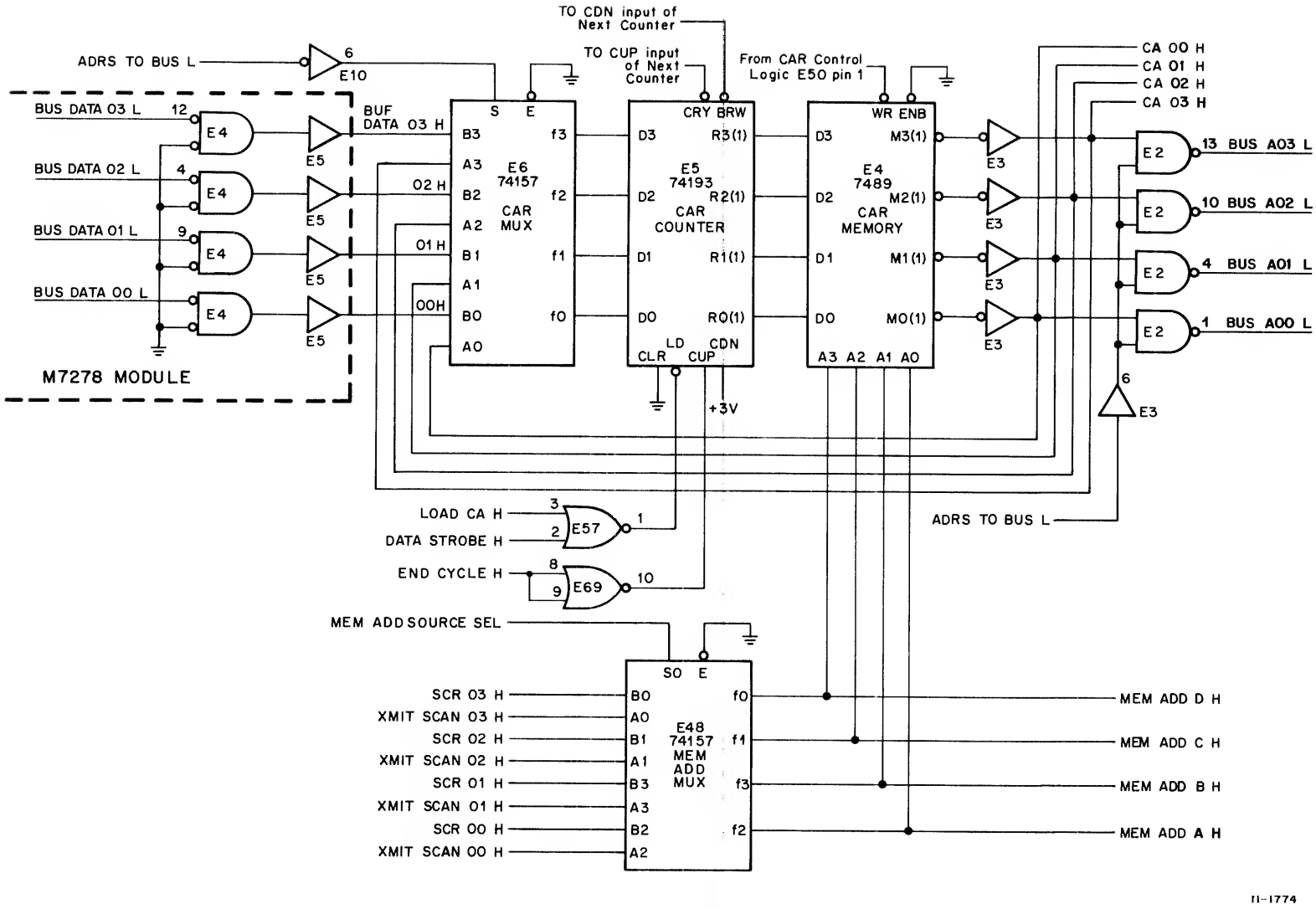


Figure 4-18 Logic Diagram of One Section (Bits 00 – 03) of Current Address Register

Figure 4-18 shows another type 74157 multiplexer (E48) whose outputs are sent to the address lines of all five type 7489 memories. This multiplexer is used because the address of the selected word has two sources: the transmitter scanner which is used during NPR transfers, and the System Control Register which is used when the program reads or writes into the CAR.

4.6.2.3 Loading the CAR – Assume that a transmit operation is to be performed and the System Control Register (SCR) has selected the desired line. The line selection bits (SCR 00 H – SCR 03 H) of the SCR are sent to the B input of multiplexer E48.

The program now desires to load the CAR with the 18-bit memory address of the first character of the message to be transmitted on the selected line. The processor addresses the CAR, asserts the Unibus control lines for a DATO transaction, and places the data on Unibus data lines D(15:00). This data represents 16 bits of the 18-bit address required. Bits 16 and 17 are determined by signals SCR 04 H and SCR 05 H from the SCR which has been previously loaded by the program. They are sent directly from the SCR to CAR multiplexer E33 (drawing D-CS-M7277-0-1, sheet 5). Unibus bits D(15:00) are picked off the bus by type 380 bus receivers, buffered, and sent to CAR multiplexers E6, E13, E20, and E27 as signals BUF DATA 00 H – BUF DATA 15 H. Signal ADDRS to BUS L is high because this is a programmed CAR load, not an NPR. It is inverted and sent to the select (S) inputs of the five CAR multiplexers. This enables BUF DATA 00 H – 15 H, SCR 04 H, and SCR 05 H to the inputs of the five counters.

The processor addressing the CAR has caused the gating control logic on the M7277 module to assert LOAD CA H. This signal is sent to the CAR control logic to provide three functions:

a. Puts a high signal (MEM ADD SOURCE SEL) on the select (S0) input of multiplexer E48 which enables the B input word (SCR 00 H – 03 H) to the output. The 4-bit binary output f0 – f3 represents the number of the line selected for address loading. This output is sent to the address lines of the 7489 memory to select the proper word into which the address is to be written.

b. Puts a low on the load (LD) input of the counter which enables the input to the output. This places the current address on the input of the CAR memory.

c. Puts a low on the write (WR) input of the memory which performs a write operation. This operation places the input data (current address) into the selected word.

The output of the memory is the complement of the data just written into it. These 18 bits are inverted and fed back to the B word input of the CAR multiplexer to be used in incrementing the CAR.

Each bit of the CAR is also inverted and sent to one input of a type 8881 Unibus driver. All 18 drivers are enabled by a common signal (ADR TO BUS L) when the DH11 is bus master. This action is described in the following paragraph.

4.6.2.4 Incrementing the CAR – Assume that the CAR has been loaded with the current address of the first character to be transmitted. The DH11 becomes bus master through an NPR in order to transfer the character from memory to the appropriate UART for transmission.

When the DH11 becomes master, signal ADRS TO BUS L is asserted by the M796 module. This signal is inverted and enables all 18 Unibus drivers to place the current address on the Unibus A lines. The current address to be applied to the Unibus A lines is selected by signals MEM ADD A H through MEM ADD D H, which are the address selection bits for the CAR 7489 memory. They are the outputs of multiplexer E48 and are enabled from the A word input because the select input (MEM ADD SOURCE SEL) is low. The A word consists of signals XMIT SCAN 00 H through XMIT SCAN 03 H from the transmitter scanner. They represent the position of the scanner or the number of the line from which the transmission is to occur.

The current address is also sent to the B word input of the CAR multiplexer. An inverted ADDRS TO BUS L signal selects this information as inputs to the CAR counter.

The M796 module asserts DATA STROBE H which enables the load (LD) input of the counter which transfers information into the counter.

The M796 module asserts END CYCLE L which is buffered and sent to the count up (CUP) input of CAR counter E5 associated with current address bits 00 – 03 (drawing D-CS-M7277-0-1, sheet 6). The counter is clocked by the positive edge of the END CYCLE L pulse. This counter is incremented by 1 and this count, if necessary, is rippled through the rest of the counters. The counter output, which is the memory input, now represents the current address plus 1. The CAR control logic provides a delayed path for the END CYCLE L pulse to the write input (WR) of the CAR memory. This input is driven low and the memory performs a write operation that places the input data (CA + 1) into the selected word. This operation is delayed to allow time for the counter outputs to settle after incrementation.

The current address has been incremented and stored awaiting the next NPR cycle. This process is repeated until the last character has been transmitted.

4.6.2.5 Reading the CAR – Assume that the program desires to read the current address on the line selected by the SCR. The processor asserts the Unibus control lines for a DATI and addresses the CAR. When the CAR address is decoded, the M7277 module asserts READ CA L, DATA TO BUS H, and DATA SOURCE AH, BH, CH.

Signal READ CA L puts a high on the select (S) input of multiplexer E48 which enables the B word input (SCR 00 H – 03 H) to the address lines of the CAR memories. This selects the desired memory word as a function of the SCR. The write (WR) input of the memory is high (disabled) which indicates a read function. This places the complement of the contents of the selected word on the memory output. All 18 bits are inverted and sent to module M7278. Bits 00 – 15 are identified as CA 00 H – CA 15 H. Bits 16 and 17 are identified as SSR 06 H and SSR 07 H, respectively.

The M7278 contains a multiplexer that multiplexes all 16 bits of the 8 DH11 registers and enables them to 16 Unibus drivers. The multiplexer consists of 16 type 74151 8-line to 1-line multiplexers. Figure 4-19 shows the select input logic and the section for bit 00 (multiplexer E43). Bit 00 from each of the DH11 registers is sent to inputs D0 – D7. Input selection is made by signals DATA SOURCE AH, BH, and CH which are sent to select inputs S0, S1, and S2, respectively. Only the 1-output (pin 05) is used. It is connected to a type 8881 Unibus driver that is enabled when DATA TO BUS H is asserted.

In this case, when the CAR address is decoded, DATA SOURCE AH, BH, and CH select input D3 and DATA TO BUS H enables this input to the Unibus. This transaction reads only BUS A 00 L – BUS A 15 L that are represented by signals CA 00 H – CA 15 H. Bits BUS A 16 L and BUS A 17 L are represented by SSR 06 H and SSR 07 H which must be read by performing a DATI on the SSR.

4.6.3 CAR Control Logic

In the previous discussion of the CAR loading, incrementing, and reading operations, certain control signals are mentioned but not described. This paragraph describes the logic that generates these signals (drawing D-CS-M7277-0-1, sheets 5 and 6). Loading the Byte Count (BC) Register is also described because it shares some of the CAR control logic, with the few exceptions that are described in Paragraph 4.7.

Figure 4-20 is a detailed diagram of the CAR control logic plus timing diagrams for the CAR loading and incrementing operations. The discussion is divided into three parts: loading the CAR, incrementing the CAR, and loading the BC register.

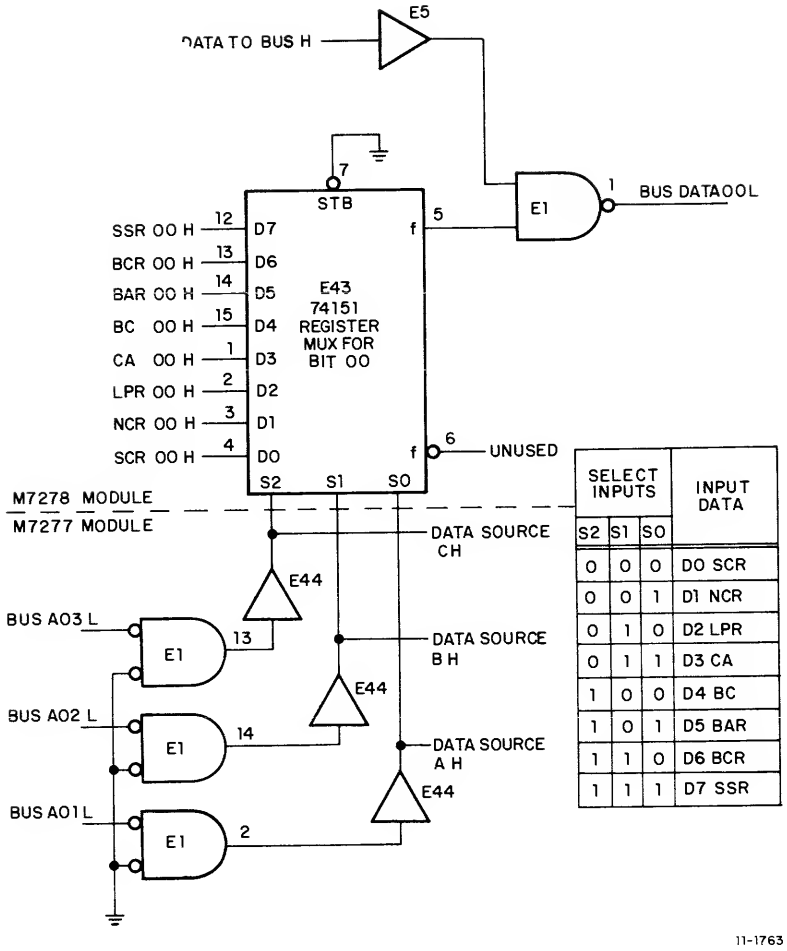


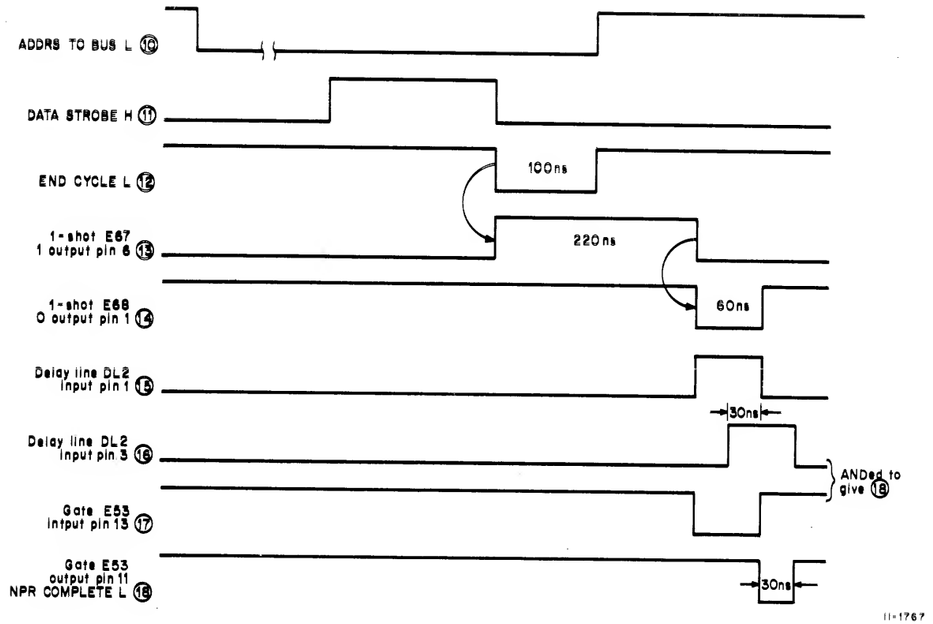
Figure 4-19 Logic Diagram for Bit 00 of Registers Multiplexer

4.6.3.1 Loading the CAR – During the CAR loading operation, as described in Paragraph 4.6.2.3, signal LOAD CA H is asserted. It is sent to pin 3 of NOR gate E57 whose output (pin 1) sends a low to the load (LD) input of the CAR counter.

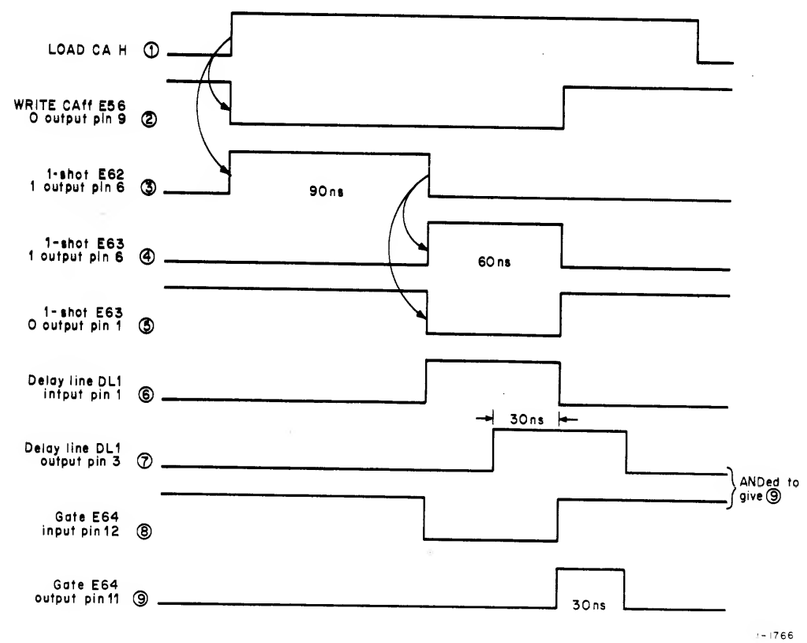
When LOAD CA H goes high, the positive transition clocks the WRITE CA flip-flop. The D input of this redefined flip-flop is connected to ground (logical 0). Therefore, it is set and its (1) L output (pin 9) is sent to E55 pin 9, where it is inverted and sent to the select (S) input of multiplexer E48. This causes the CAR memory address lines to be connected to signals SCR 00 H – SCR 03 H.

The (1) L output (pin 9) of the WRITE CA flip-flop is also sent to pin 12 of gate E50. This low signal partially qualifies E50; its other input (pin 11) is connected to the 0-output of one-shot E63 which is high because E63 is not triggered.

LOAD CA H is inverted by pins 11 and 13 of gate E57 and sent to the input (pins 3 and 4) of one-shot E62. The negative edge at this input triggers E62. A 90 ns positive pulse is produced at the 1-output (pin 6) of E62 and is sent to the input (pins 3 and 4) of one-shot E63. When the 90 ns pulse times out, the negative edge triggers E63. A 60 ns negative pulse is produced at the (1) L output (pin 1) of E63 and is sent to pin 11 of E50. This qualifies E50 and its high output (pin 13) is inverted by another E50 gate and sent to the write (WR) input of the CAR memory. This signal is delayed approximately 90 ns from the time that LOAD CA H goes high, allowing the buffered data leads to settle at the inputs of the CAR location selected by SCR 00 H – SCR 03 H.



Timing Diagram For Incrementing Operation



Timing Diagram For Loading Operation

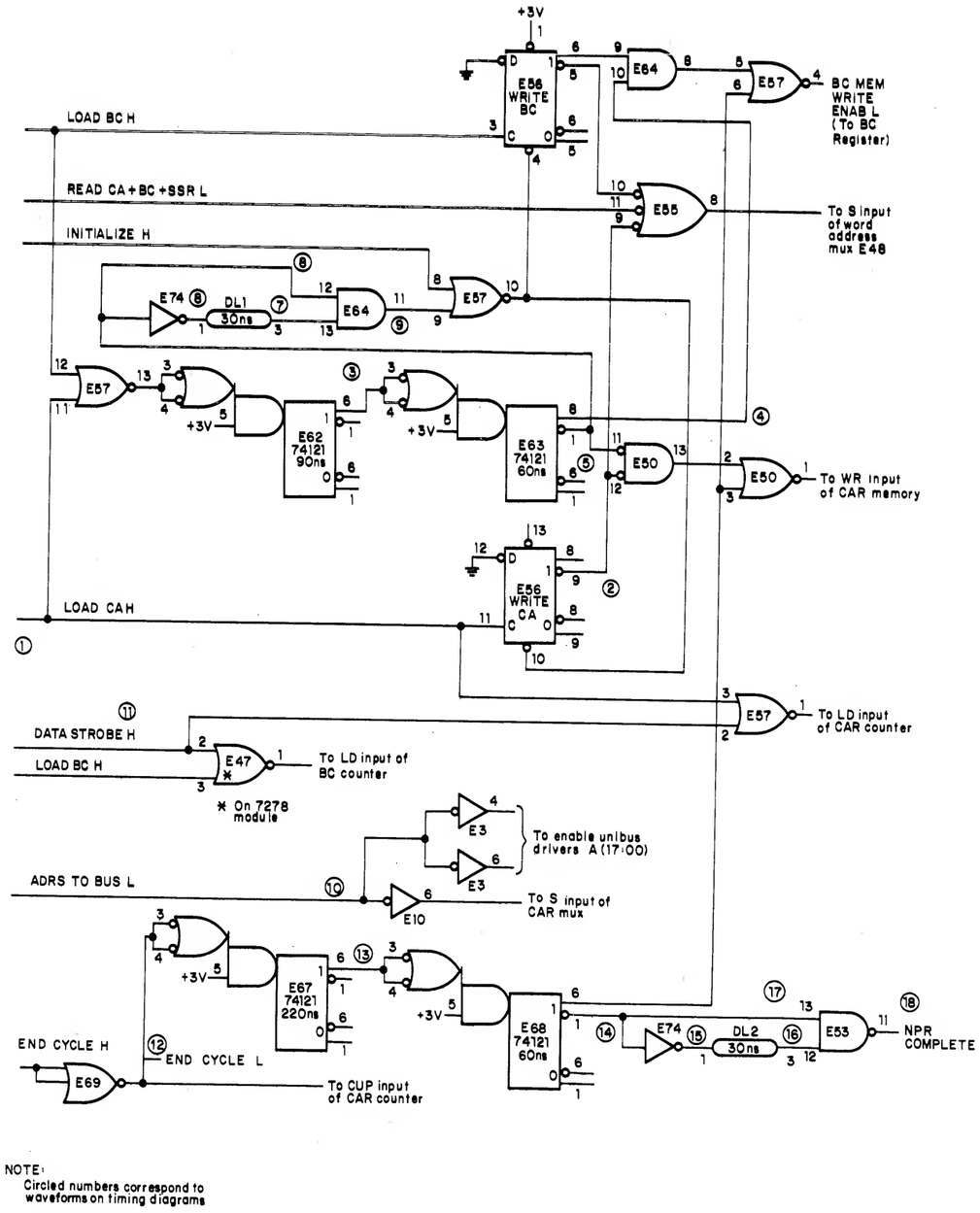


Figure 4-20 CAR Control Logic and Timing Diagrams

The (1) L output of one-shot E63 is also sent to the input of a pulse generator consisting of inverter E74, 30 ns delay line DL1, and 2-input AND gate E64. The output (pin 11) of E64 is low when one-shot E63 is not triggered and during the period that E63 is triggered. However, when E63 times out, and for 30 ns after, E64 pin 11 is high. This signal is inverted by E57 and sent to the clear input (pin 10) of the WRITE CA flip-flop.

4.6.3.2 Incrementing the CAR – During the CAR incrementing operation, the M796 module asserts three signals: ADDRS TO BUS L, DATA STROBE H, and END CYCLE L. Refer to the timing diagram for the incrementing operation shown in Figure 4-20.

ADDRS TO BUS L, is asserted first, inverted by E3 pins 3 and 4 and E3 pins 5 and 6 to enable the current address to the Unibus. It is also inverted by E10 pins 5 and 6 and sent to the select (S) input of the CAR multiplexer, to connect the CAR memory outputs to the CAR counter inputs.

DATA STROBE H is asserted next and inverted by E57 pins 2 and 1. This low signal is sent to the load (LD) input of the CAR counter, thus loading the current address into the counter.

END CYCLE H is asserted last, inverted by E69, and sent to the count up (CU) input of the CAR counter. This signal is also sent to the input (pins 3 and 4) of one-shot E67. The negative edge at this input triggers E67. A 220 ns positive pulse is produced at the 1 output (pin 6) of E67 and sent to the input (pins 3 and 4) of one-shot E68. When the 220 ns pulse times out, the negative edge triggers E68. A 60 ns positive pulse is produced at the 1-output (pin 6) of E68. It is inverted by E50 pin 1 and sent to the write (WR) input of the CAR memory. This signal is delayed approximately 220 ns from the time that END CYCLE H is asserted to allow time for the CAR counter to reach the incremented address before the 60 ns pulse writes that value into the CAR location.

The 60 ns negative pulse from the (1) L output of one-shot E68 is sent to the input of a pulse generator consisting of inverter E74, 30 ns delay line DL2, and 2-input NAND gate E53. This circuit operates like the one described in the CAR load operation. It produces a 30 ns negative pulse at E53 pin 11 which is NPR COMPLETE L and is used to restart the transmitter scanner.

4.6.3.3 Loading the BC Register – Most of the CAR control logic used in the CAR loading operation is used in the BC register loading operation. An additional flip-flop (WRITE BC) and three gates are used exclusively for the BC operations.

When LOAD BC H goes high, the positive transition clocks the WRITE BC flip-flop. The D input of this redefined flip-flop is connected to ground (logical 0); therefore, it is set and output (1) L (pin 5) is low. This signal is sent to pin 10 of E55, inverted and sent to the select (S) input of the memory address multiplexer (E48) whose outputs are also used by the BC register memory to select the byte count for the line indicated by signals SCR 00 H – SCR 03 H.

During the BC loading operation, signal LOAD BC H is asserted. It is sent to pin 2 of NOR gate E47 which is located on the M7278 module. The signal is inverted by E47 and sent to the load (LD) input of the BC counter to load the present byte count into the byte count counter.

The (1) H (pin 6) output of the WRITE BC flip-flop is high. This signal is sent to pin 9 of 2-input AND gate E64. The other input (pin 10) of E50 is qualified when one-shot E63 is triggered. The sequence for triggering E63 is the same as that described in the CAR loading operation except that the sequence is initiated by LOAD BC H rather than LOAD CA H. The high output (pin 8) of E50 is inverted by E57 pins 5 and 4 and sent to the write input (WR) of the BC memory as signal BC MEM WRITE ENAB L. Again E62 produces a 90 ns delay to allow for the byte count memory data selection and counter loading action described in the previous two paragraphs.

As in the case of the CAR loading operation, when E63 times out, a 30 ns positive pulse is produced at the output (pin 11) of E64. It is inverted by E57 pins 9 and 10 and sent to the clear input (pin 4) of the WRITE BC flip-flop which clears it.

4.6.4 High Byte/Low Byte Selection Logic

When the DH11 becomes bus master and performs a DATI operation, the 18-bit current address is enabled to Unibus address lines A(17:00). This address specifies a byte (8 bits) of information stored in memory. A low byte consists of data bits D(07:00) and it has an even address (last binary digit is 0). A high byte consists of data bits D(15:08) and it has an odd address (last binary digit is 1). The byte, which is the character to be transmitted, must be taken off the Unibus data lines and sent to the selected UART. The byte control logic selects the proper byte but before it is sent to the UART it passes through another multiplexer. This multiplexer is controlled by the auto-echo circuit. During normal operation, it allows the selected byte from memory to pass to the UART for transmission. During the auto-echo mode of operation, it allows received data to pass to the UART for transmission back to the source.

The byte control logic is shown in Figure 4-21 and drawing CS-D-M7277-0-1, sheet 6. In this discussion, and as shown in Figure 4-21, the auto-echo selection logic is also included.

Byte identification is determined by sampling the least significant bit (00) of the CAR. Physically, the sampling is made at the bit 00 output of the CAR memory (E4 pin 5). This bit is connected to pin 5 of gate E50. The other input (pin 6) of this gate is ADDRS TO BUS L, which enables the current address to the Unibus A lines. The output (pin 4) of E50 is connected to the select (S) input of the byte selection multiplexer that consists of two type 74157 quad 2-line to 1-line multiplexers (E40 and E43). When the select (S) input is low, input word A or the low byte is selected; when the select (S) input is high, input word B or the high byte is selected.

Assume that bit 00 of the CAR is a 0 (low) which indicates an even memory address (low byte). This is the actual state of the bit as stored in the CAR memory. When it is read out, the complement of bit 00 appears at E4 pin 5. ADDRS TO BUS L is low at this time because it is gating the current address to the Unibus A lines. Under these conditions, E50 pin 5 is high and E50 pin 6 is low. The output (pin 4) of E50 is low which selects input word A or the low byte of the multiplexer (E40 and E43). BUFF DATA 00 H – 07 H are sent to input word B of the AE multiplexer which is also composed of two type 74157 quad 2-line to 1-line multiplexers (E39 and E42). Input word A of the AE multiplexer consists of the eight received data bits of the UART selected for operation in the auto-echo mode. The select input of the AE multiplexer is connected to AE GO L which is high when the auto-echo mode is not enabled. Such is the case in this example. With the select (S) input high, the B word is selected by the AE multiplexer; this is BUFF DATA 00 H – 07 H.

These bits are sent to the transmitter Data Holding Register for the selected UART. This byte is now identified as TRAN DATA 1 H – 8 H.

With the auto-echo feature enabled, AE GO L is low and input word A is selected. This word represents the eight bits of the selected UART data out lines that are to be transmitted back to the source.

These bits come from the output of eight 2-input NOR gates (4 each E38 and E41). Each gate has two inputs: one is UC1 RCV DATA XL and the other is UC2 RCV DATA XL. Signal UC1 RCV DATA XL represents a specific bit from the received data bus on one UART card (UC1). Signal UC2 RCV DATA XL represents the same bit on the other UART card (UC2). Each of these signals represents the bussing of eight RCV DATA X lines from the eight RCV DATA X lines from the eight UARTs on the card; together, they represent the RCV DATA X lines of all 16 UARTs. During a receiving sequence, only one UART has its Received Data Enabled.

4.7 BYTE COUNT REGISTER

4.7.1 Introduction

The Byte Count (BC) Register and associated output logic are located on the M7278 Byte Count and Master Registers Module (drawing D-CS-M7278-0-1, sheets 3 and 4). The BC register is loaded similarly to the CAR and shares the CAR control logic. The BC register is incremented in the same way and at the same time that the CAR is incremented.

Because the BC register is functionally similar to the CAR, this discussion deals primarily with the unique features of the BC register.

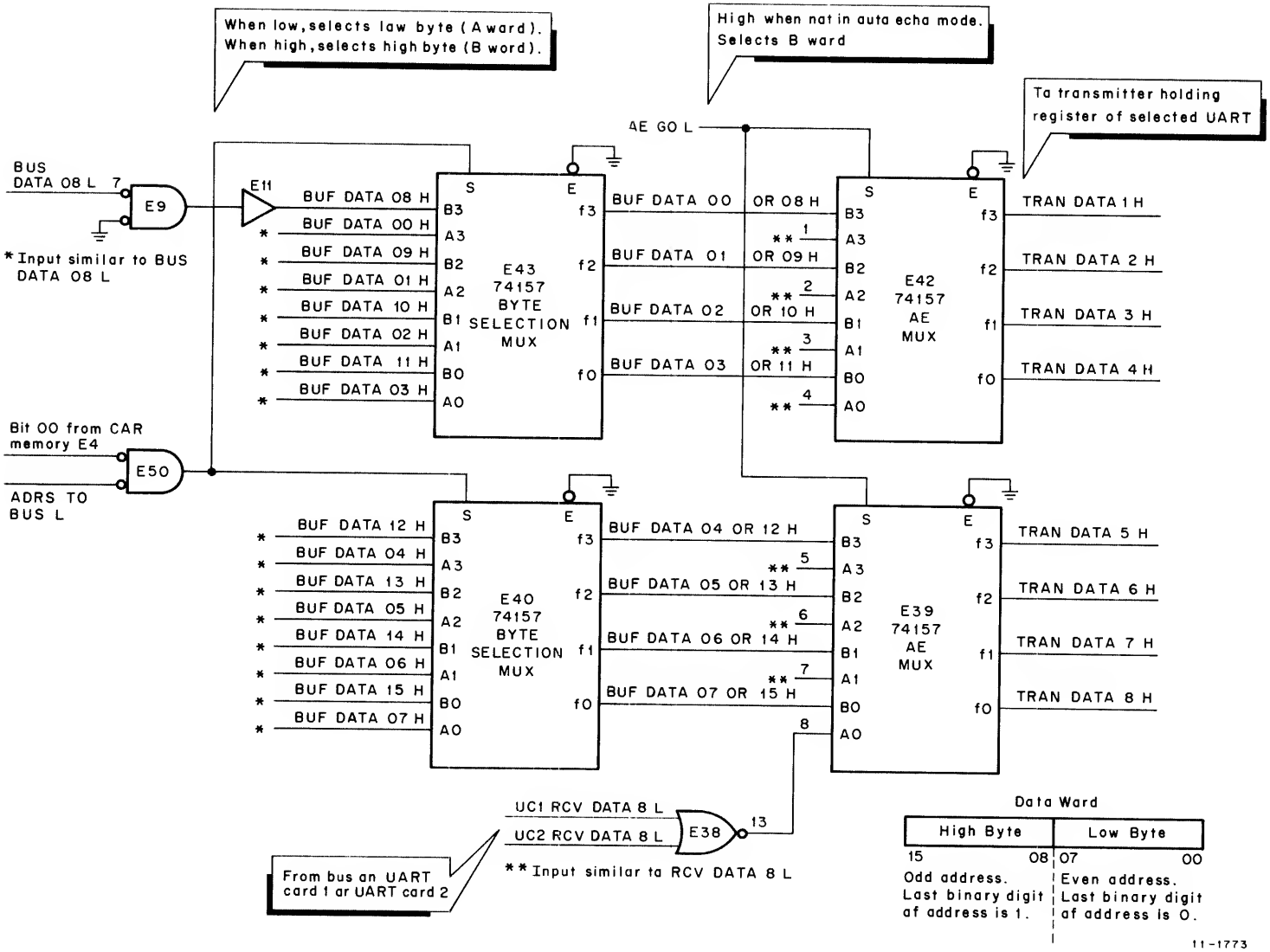


Figure 4-21 Byte Control Logic

4.7.2 Byte Count Register

4.7.2.1 Functional Description – In the transmit mode, the program loads the BC register with the 2's complement of the number of characters (bytes) to be transmitted. This may be done by means of a MOV #- N, BC instruction, where N = number of characters to be transmitted and BC is the address of the Byte Count Register. SCR 00 – SCR 03 must first be selected for the appropriate line. During each NPR transaction that brings a character from memory to the DH11, the BC register is incremented. The BC counter is counting the number of characters transferred. Because it has been loaded with the 2's complement of the number of characters, the BC counter increments towards overflow which it reaches when the desired number of characters have been transferred. At overflow, the BC register output logic generates a signal that clears the BAR bit for the selected line. This indicates that the last character to be transmitted on that line has been loaded into the transmitter Holding Register of the associated UART.

4.7.2.2 Components – The BC register consists of the following major components (drawing D-CS-M7278-0-1, sheets 3 and 4):

a. Four type 7489 64-bit read/write memories (E31, E32, E33, and E34) with common address lines and enabling inputs organized to form a 16-word by 16-bit memory.

b. Four type 74193 synchronous 4-bit counters (E24, E25, E26, and E27) cascaded to form a 16-bit counter.

c. Four type 74157 quad 2-line to 1-line multiplexers (E16, E17, E18, and E19) with a common select signal to provide a 16-bit multiplexer.

The interconnection and function of these devices are the same as those used in the CAR and described in Paragraph 4.6.2.2.

4.7.2.3 Loading and Incrementing the BC Register – The BC register is loaded with the 2's complement of the number of characters (bytes) to be transmitted. This allows the BC counter to be preset to a count that is less than overflow by the number of characters selected. During each NPR, the counter is incremented and when the last character is transferred it overflows.

The overflow is used to generate a signal that clears the BAR bit for the selected line. This action is described in the following paragraph.

4.7.2.4 BC Register Output Logic – The logic that uses the counter overflow to clear the BAR bit is shown in Figure 4-22 and drawing D-CS-M7278-0-1, sheet 3.

When the BC counter overflows, all 16 outputs (bits 00 – 15) are 0. These 16 signals are sent to four type 8815 4-input NOR gates (E22 and E23) that are shown symbolically as logically equivalent negated input AND gates. The high output of each of these gates is sent to an input of 4-input NAND gate E15. The output of E15 is driven low and this negative transition triggers one-shot E14. A 40 ns negative pulse (XMIT FINISHED PULSE L) is generated at the (1) L output (pin 1) of E14 and sent to both strobe inputs (STB0 and STB1) of E48 which is a type 74154 4-line to 16-line decoder. The low signals on inputs STB0 and STB1 enable E48, and 1 of 16 mutually-exclusive outputs is decoded from BCD inputs D0 – D3. These decoding signals are MEM ADD A H through MEM ADD D H from the memory address multiplexer (E48) on the M7277 module. These address lines are the same ones that select the byte count memory location and represent the transmitter scanner position or the line being serviced. The appropriate low output from decoder E48 is sent to one input of a type 7408 2-input positive AND gate which is shown symbolically as a logically equivalent negative OR gate. The other input to the 7408 gate is the inversion of INIT B H which is high because INIT B H is low (not asserted) at this time. The 7408 output is low and a CLR BAR XX L signal is asserted. This signal clears the BAR bit for the selected line.

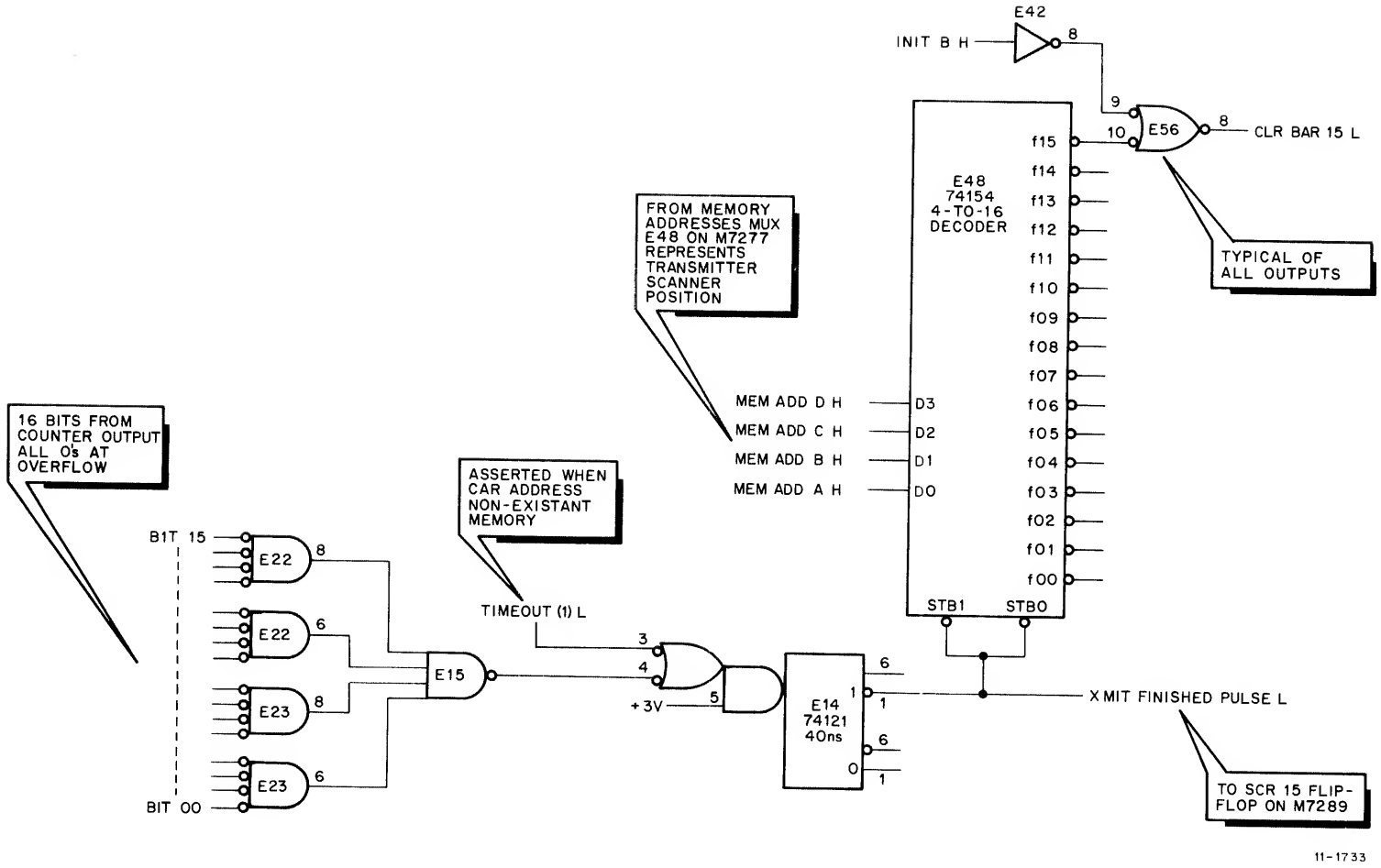


Figure 4-22 BC Register Output Logic

A selected BAR bit is cleared also when TIMEOUT (1) L is asserted at the input of one-shot E14. This occurs when the current address logic tries to address non-existent memory.

The 40 ns XMIT FINISHED PULSE also sets bit 15 of the System Control Register. In normal DH11 operation, only this pulse sets SCR 15 to generate a transmit complete interrupt (if enabled). Clearing the BAR bit by program action does not set SCR 15 or generate an interrupt. Clearing the byte count by program action does generate XMIT FINISHED PULSE, clear SCR 15, and generate the interrupt. Therefore, the latter course of action (setting BC to 0) is the recommended procedure for aborting transmission.

4.8 RECEIVER SCANNER

4.8.1 Introduction

The receiver scanner logic is located on the M7289 System Control and Receiver Scanner Module (drawing D-CS-M7289-0-1, sheets 3 and 4). This discussion is divided into three major parts:

a. Basic operation of the receiver scanner and receiver sequencer

b. Operation of the status sampling logic

c. Operation of the auto-echo feature.

4.8.2 Receiver Scanner and Receiver Sequencer

This discussion first covers operation of the receiver scanner and receiver sequencer in servicing a character. Assume that the silo can accept a character and data is available on the selected line.

The major component of the scanner is counter E25 (drawing D-CS-M7289-0-1, sheet 3). It is a type 74193 synchronous 4-bit up/down counter. In this application it is connected to count up by sending FREQUENCY DIVIDE clock pulses to the count up (CUP) input while the count down (CDN) input is held high. The data inputs are not used (D0 – D3 connected to ground) and the load (LD) input is permanently held inactive by connecting it to +3 V. The counter cannot be preset so it counts up from decimal 0 – 15, overflows (returns to 0), and continues upcounting and overflowing as long as clock pulses are supplied. The counter outputs are buffered by type 7417 non-inverting buffers and sent to both M7280 UART Modules as RCV SCAN leads. They are identified as RCV SCAN A, RCV SCAN B, RCV SCAN C, and RCV SCAN D which is the most significant bit. These signals are sent to several decoders on the UART cards. In this case, the appropriate one is E18 which is a type 74151 data selector (drawing D-CS-M7280-0-1). E18 is shown in Figure 4-23. The eight inputs to E18 are BUF DA LINE 0 – BUF DA LINE 7. Each signal is from the received data available output of each UART on the card. This output goes high when a character has been received and transferred to the UART receiver Holding Register. Signal RCV SCAN D is sent to the strobe (STB) input of decoder E18 which enables it. Signals RCV SCAN C, RCV SCAN B, and RCV SCAN A are sent to the select inputs (S2, S1 and S0) of E18. These inputs select 1 of the 8 inputs to E18. As it counts, the scanner counter, through its outputs (RCV SCAN lines), scans the eight BUF DA LINE signals. If a selected UART has received data available, its BUF DA LINE goes high, which in turn drives the output of E18 (MASTER DA) high. MASTER DA is sent to the receiver scanner logic. The function of MASTER DA is described subsequently.

At this point, the discussion digresses to explain a note concerning the Receiver Scan D signal on drawing D-CS-M7289-0-1, sheet 3. The drawing shows both D and its inversion D with a note that one UART card uses D and the other uses D. The reason for this arrangement is shown graphically in Figure 4-24. The example shows only the DA line decoders but it is applicable to the other decoders on the UART cards.

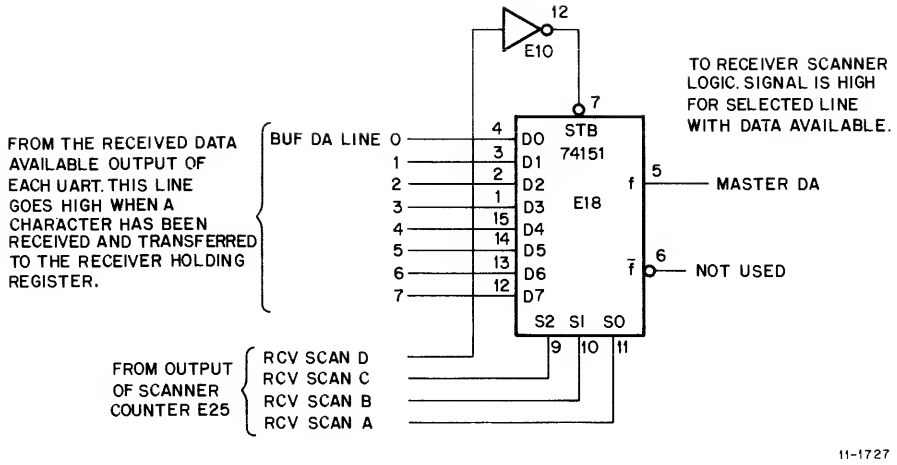


Figure 4-23 UART Data Available Line Decoder

Each UART card contains eight UARTs whose DA lines are decoded by a type 74151 data selector (E18) that uses the RCV SCAN outputs from the receiver scanner counter for enabling and selection. By sending the RCV SCAN D signal to one UART card and the inverted RCV SCAN D signal to the other UART card, each E18 decoder is enabled for a successive 8 count sequence from 0 – 7. This allows interchangeability of the two UART cards in their assigned slots.

The discussion now returns to the operation of the receiver scanner logic. As previously mentioned, counter E25 is clocked by signal FREQUENCY DIVIDE. This signal has a frequency of 633 kHz and is obtained by performing a divide by 4 function on the 2.534 MHz signal from counter E05 on the M4540 Clock Module. The 2.534 MHz signal is sent to the clock input of FREQ DIV A flip-flop (drawing D-CS-M7289-0-1, sheet 4). The (0) H output of FREQ DIV A is fed back to its D input so that the flip-flop changes state at each positive edge of the clock pulse. This produces complementary signals at the FREQ DIV A flip-flop outputs that have a frequency of 1.267 MHz. The (1)H output of FREQ DIV A is TRAN SCAN CLK H which is sent to module M7277 to clock the FREQ DIV C flip-flop in the transmitter scanner logic. The (0)H output of FREQ DIV A is used to clock the FREQ DIV B flip-flop. The (0)H output of this flip-flop is fed back to its D input through 2-input AND gate E40. Assume that the other input of E40 remains high. This produces complementary signals at the FREQ DIV B flip-flop outputs that have a frequency of 633 kHz. The (1)H output of this flip-flop is the FREQUENCY DIVIDE signal that clocks the receiver scanner counter (E25). The positive edge of the signal is used to clock the counter and this occurs when FREQ DIV B is set (goes to 1 state). When FREQ DIV B is reset cleared, delay network (DL2 and E40) generates a 30 ns positive pulse at E40 pin 3. As FREQ DIV B flip-flop toggles, it generates a positive 30 ns pulse approximately every 1.6 μs. These pulses are used to clock the SCAN STOP flip-flop. The state of this flip-flop is determined by its D input which is a function of received data available in a selected UART and space available in the silo. The functions are sensed at inputs 9 and 10 of AND gate E30 whose output (pin 8) is sent to the D input of the SCAN STOP flip-flop.

Determination of the availability of received data is indicated by the MASTER DA H signal from UART card number 1 or 2. UC1 MASTER DA H from UART card 1 and UC2 MASTER DA H from UART card 2 are ORed at gate E9 pins 5 and 6. If the scanner samples a selected line which has its Received Data Available flag high, one of the two MASTER DA H signals is asserted. It is double inverted by E9 and E5 and sent as a high signal to pin 10 of E40.

Determination of space available in the silo is indicated by the READY IN L signal from the silo (M7279 module). READY IN L is asserted (low) when space is available. When READY IN L goes from high to low, the delay network (E33, DL1, and E40) generates a 30 ns positive pulse at E40 pin 11 that clocks the SILO READY flip-flop. This

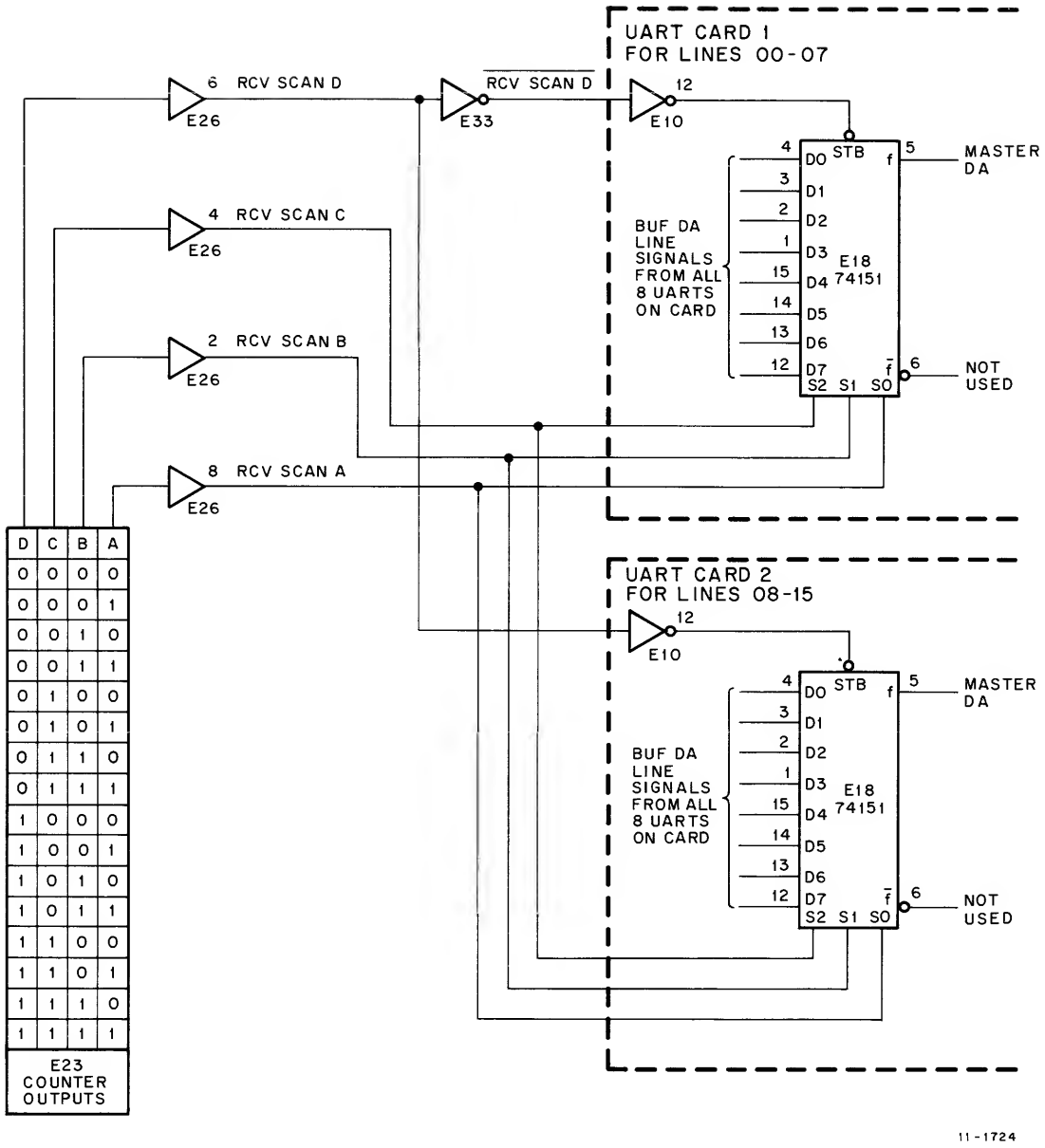
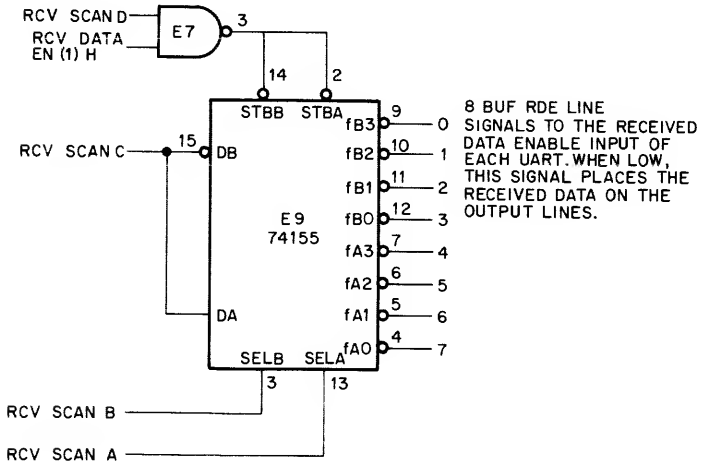


Figure 4-24 Receiver Scan Lines to UART Cards

redefined flip-flop is set and its (1)H output puts a high on pin 9 of E40. The other input (pin 10) of E40 is already high so its output (pin 8) goes high. This places a high on the D input of the SCAN STOP flip-flop which sets when the next 30 ns clock pulse arrives. The (0)H output of SCAN STOP puts a low on pin 4 of E40 which in turn puts a low on the D input of FREQ DIV B. This action prevents FREQ DIV B from toggling and holds it in the 0 state. The clock signal (FREQUENCY DIVIDE) for counter E25 is inhibited and the counter stops. The receiver scanner is now stopped and is pointing to the line that has a UART with received data available.

With SCAN STOP set, its (1)H output puts a high on pin 11 of 3-input NAND gate E43. Assume that the other two inputs of this gate are high also. This requires that the RESTA SCAN flip-flop is not set; ABANDON L is not asserted; and flip-flop R0(1) in E21 is not set. The output (pin 8) of E43 is low and is sent to the D input of the redefined RECV DATA flip-flop. On the next positive transition of the 2.5 MHz clock, RECV DATA is set and its (1)H output is high. This signal is RECV DATA EN (1)H and is sent to the UART card as an enabling signal for the received data enable decoder (E9). This device is a type 74155 dual 2-line to 4-line decoder that is connected to operate as a 3-line to 8-line decoder. Figure 4-25 contains a block diagram, truth table, and notes that describe the operation of decoder E9. The four RCV SCAN outputs (D, C, B, A) from the receiver scanner counter are the select inputs for decoder E9. Since the scanner has been stopped, these lines point to the selected UART that has received data available. When RECV DATA EN (1) H is asserted, decoder E9 asserts the proper BUF RDE LINE signal at its output. This low signal is sent to the STB RD input (pin 4) of the appropriate UART and places the received data onto the UART received data bus as BUF RCV DATA 01 – BUF RCV DATA 08. These data bits are sent to the silo input to await subsequent loading into the silo.

Signal RECV DATA EN (1) H also initiates operation of the receiver sequence that performs a series of functions in sequence, terminating with a silo load operation and restart of the receiver scanner. Before discussing the sequencer, let us back track and examine the operation of the scanner logic in the event that the selected UART did not have received data available or the silo was full.



TRUTH TABLE

SEL				OUTPUTS							
C	B	A	STB	0	1	2	3	4	5	6	7
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

X = IRRELEVANT

NOTES:
1. Device is connected os o 3-line to 8-line decoder.
2. Third select line (C) is obtoined by connecting inputs DA ond DB together.
3. Strobes ore connected together for enobling.

11-1725

Figure 4-25 UART Received Data Enable Decoder

If the selected line does not have received data available, both UC1 MASTER DA H and UC2 MASTER DA H are low. The output (pin 4) of NOR gate E9 is high. It is inverted by E5 and sent to pin 10 of AND gate E40. This gate is disqualified and its low output is sent to the D input of the SCAN STOP flip-flop. This holds SCAN STOP in the 0 state and the scanner continues to operate.

If the selected line has received data available (MASTER DA H is asserted) and the silo is full, the scanner continues to operate but signal STORAGE OVERFLOW L is generated to indicate a full silo.

Under these conditions, READY IN L from the silo logic is high which indicates no available space in the silo. This prevents clocking of the SILO READY flip-flop so it remains in the 0 state. The (1)H output of SILO READY disqualifies AND gate E40 and thus holds the SCAN STOP flip-flop in the 0 state. The scanner continues to operate, so 30 ns positive pulses are produced at E40 pin 3 which is connected to E43 pin 1 as well as to the SCAN STOP flip-flop clock input. When a 30 ns positive pulse appears at E43 pin 1, all three inputs are high which drives its output (pin 12) low to produce a STORAGE OVERFLOW L pulse. This signal is sent to the present input (pin 10) of the SCR 14 flip-flop in the System Control Register (drawing D-CS-M7289-0-1). This is the storage interrupt flag (bit 14) of the SCR. When set, this bit causes an interrupt if the SCR storage interrupt enable bit (12) is also set.

The discussion now returns to the point at which RECV DATA EN (1) H is enabled and the received data bits are at the silo input to await subsequent loading into the silo. The RECV DATA EN (1) H is sent to pin 1 of AND gate E17 to initiate operation of the receiver sequencer.

The receiver sequencer consists of one type 74174 hex flip-flop package E21, six 2-input AND gates and two output inverters (drawing D-CS-7289-0-1, sheet 4). Assume that signal ABANDON L is not asserted and the six sequencer flip-flops (E21) are cleared. These conditions drive E13 pin 11 high which puts a high on one input of the six sequencer input AND gates (E17 pin 2, E17 pin 4, E17 pin 13, E17 pin 9, E13 pin 1, and E13 pin 4). Signal RECV DATA EN (1) H has been asserted and sent to pin 1 of gate E17. The other input (pin 2) is also high so its output (pin 3) goes high. This signal is sent to the D5 input of E21. The next 2.5 MHz clock pulse sets flip-flop 5 and its output R5 (1) goes high. This signal is sent to E17 pin 5 which is the input AND gate for flip-flop 4. It puts a high on D4 and this flip-flop is set on the next 2.5 MHz clock pulse. Similar connections allow flip-flops 3, 1, 2, and 0 to set on successive 2.5 MHz clock pulses. Figure 4-26 is a timing diagram for the receiver sequencer.

We are still discussing the operation of the receiver scanner in servicing a character. Auto-echo is not enabled and the hardware requires only a signal to load the silo and start the receiver scanner. SAMPLE STATUS H is the first signal generated by the sequencer and has no effect on this operation.

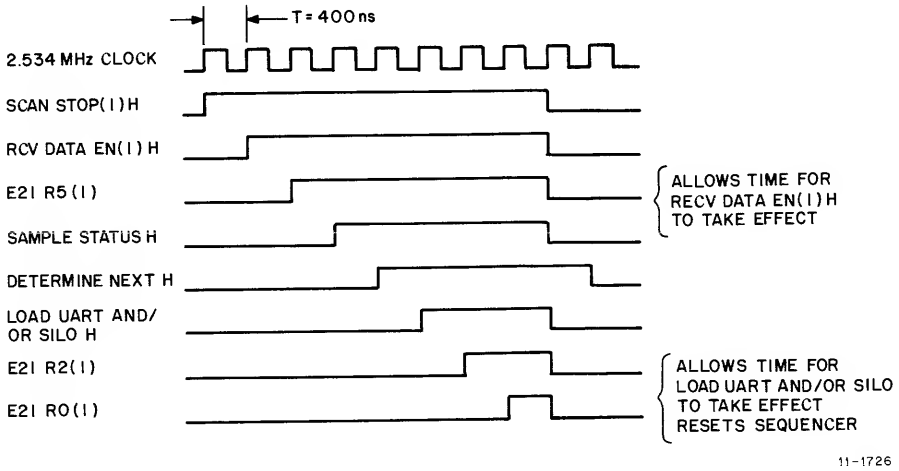


Figure 4-26 Timing Diagram for Receiver Sequencer

DETERMINE NEXT H is asserted next and is sent to three E2 NAND gates (drawing D-CS-M7289-0-1, sheet 3). The gate under consideration in this case is E2 pin 10. The other input (pin 9) of this gate is high also because auto-echo is not enabled. E2 pin 8 goes low and is sent to pin 12 of E1. LOAD UART AND/OR SILO L is asserted by the sequencer and sent to the other input (pin 11) of E1. The output (pin 13) of E1 goes high and is inverted by another E1 gate. The output of this gate (pin 10) is LOAD SILO L and is sent to the silo logic to initiate a silo load operation. The high output of E1 pin 13 is RESET DATA AVAIL H and is sent to the UART boards to clear the Data Available flag on the selected line. When flip-flop 0 of the sequencer sets, its high output is inverted by E5 pin 2 which drives the output (pin 11) of E13 low. This disqualifies all the sequencer input AND gates; disqualifies E43 and puts a high on the D input of RECV DATA, and puts a low on the D input of RESTA SCAN. On the next 2.5 MHz clock pulse, all five sequencer flip-flops (0, 1, 2, 4, and 5) are reset; RECV DATA is reset which clears RECV DATA EN (1) H; and RESTA SCAN is set and its (1) L output directly clears SCAN STOP which starts the receiver scanner. The received character has been serviced and the receiver scanner has resumed operation. After 400 ns DETERMINE NEXT H (sequencer flip-flop 3) is cleared which allows appropriate data hold time for auto-echo hardware to load the UARTs.

4.8.3 Status Sampling Logic

The SAMPLE STATUS H signal that is asserted by the receiver sequencer is used to clock two type 74175 quad flip-flop packages E10 and E18. Six of the eight flip-flops in these two packages sample various conditions in the DH11 hardware. The status of the conditions is stored in the flip-flops and their outputs are sent to control logic associated with the receiver scanner. These status signals are used primarily to condition the control logic prior to assertion of the DETERMINE NEXT H signal when using the auto-echo feature.

This discussion covers the generation and purpose of the status signals. Their use in the receiver scanner logic is described in Paragraph 4.8.4.

The following conditions are sampled.

Master Overrun (E18 input D0)

A UART generates a high BUF OR LINE signal if the previously received character is not read (BUF DA LINE not reset) before the present character is transferred to the receiver Holding Register. The BUF OR LINE signal from each UART on a card is sent to a type 74151 data selector (E15) that is operated by the outputs of the receiver scanner counter. When the scanner stops, these leads (RCV SCAN A – RCV SCAN D) point to the selected line. The BUF OR LINE signal associated with the selected line is enabled to the data selector output as MASTER OR. There are two such signals: UC1 MASTER OR for card 1, and UC2 MASTER OR for card 2. These two signals are sent to the receiver scanner logic (drawing D-CS-M7289-0-1, sheet 3). They are ORed at E9 pins 2 and 3. The output of E9 is inverted by E5 and sent to the D0 input of E18. If the selected line indicates an overrun condition, MASTER OR is high and D0 is high. The positive edge of the SAMPLE STATUS H pulse sets the flip-flop. Conversely, the flip-flop is reset if there is no overrun condition.

Auto-Echo (E18 input D1)

Auto-echo is enabled by setting bit 15 of the LPR of the selected line. When selected, a flip-flop on the M7288 LPR module is set and it sends an AE ENAB XXH signal to type 74150 multiplexer E12 in the receiver scanner logic. Selection is provided by the receiver scanner counter leads (RCV SCAN A – RCV SCAN D) which point to the selected line. If auto-echo is enabled for the selected line, the multiplexer output is low. If auto-echo is not enabled, the multiplexer output is high. This output is sent to input D1 of E18. When clocked by SAMPLE STATUS H, this flip-flop is set when auto-echo is not enabled and it is reset when auto-echo is enabled.

Transmitter Scanner (E18 input D2)

The operating status of the transmitter scanner is required because auto-echo is not allowed if that scanner is stopped.

The status of the scanner is indicated by signal XMIT STATUS L. This signal is low if the scanner is stopped and it is high if the scanner is operating. This signal is sent to input D2 of E18. When clocked by SAMPLE STATUS H, this flip-flop is set when the scanner is operating and it is reset when the scanner is stopped.

Transmitter Buffer (E18 input D3)

The status of the Data Holding Register must be known because, during auto-echo operation, a received character is loaded in the UART for transmission back to the sending location.

A UART generates a high TMBT LINE signal when the Data Holding Register can be loaded with a character. All 16 UARTs send their TMBT LINE XXH signals to the inputs of a type 74150 multiplexer (E30) in the receiver scanner logic. Selection is provided by the receiver scanner counter leads (RCV SCAN A – RCV SCAN D) which point to the selected line. If the Data Holding Register can accept a character, the multiplexer output is low. If the register contains a character, the multiplexer output is high. This output is sent to input D3 of E18. When clocked by SAMPLE STATUS H, this flip-flop is set when the Holding Register is full and is reset when the register is empty.

Bus Request (E10 input D0)

The status of REQUEST BUS (1) H must be known because auto-echo is not allowed if an NPR cycle is in process or is being requested. During auto-echo, a received character is loaded into the UART Holding Register via the eight BUF TRAN DATA lines. These same lines are used during an NPR to bring a character from memory to the UART Holding Register. It is not desirable to attempt auto-echo and programmed transmission on the same line simultaneously. REQUEST BUS (1) H is generated by the transmitter scanner logic and is high when the DH11 is requesting the bus to perform an NPR cycle. It stays high during the NPR cycle. REQUEST BUS (1) H is sent to input D0 of E10. When clocked by SAMPLE STATUS H, this flip-flop is set when an NPR cycle is in process or is being requested, and it is reset when an NPR is not in process nor being requested.

Master Framing Error (E10 input D2)

A UART generates a high BUF FE LINE signal if the received character has a framing error; that is, if it does not have a valid stop bit. The BUF FE LINE signal from each UART on a card is sent to a type 74151 data selector (E16) on the M7280 UART card that is operated by the outputs of the receiver scanner counter. The BUF FE LINE signal associated with the selected line is enabled to the selector output as MASTER FE. There are two such signals, UC1 MASTER FE for UART card 1 and UC2 MASTER FE for UART card 2. These two signals are sent to the receiver scanner logic. They are ORed at E1 pins 2 and 3. The output (pin 1) of E1 is inverted by E9 and sent to the D2 input of E10. If the selected line has a framing error, MASTER FE is high and D2 is high. Under these conditions, SAMPLE STATUS H sets the flip-flop. Conversely, the flip-flop is reset if there is no framing error.

Table 4-5 lists the states of flip-flops E18 and E10 for the various conditions sampled.

4.8.4 Auto-Echo Feature

4.8.4.1 Introduction – The auto-echo feature is discussed here because it is closely related to the operation of the receiver scanner. The first part of the discussion covers the normal operation of the auto-echo feature. The second part discusses how auto-echo, when enabled, can be abandoned if certain qualifying conditions are not satisfied.

4.8.4.2 Functional Description – The auto-echo feature allows received characters to be transmitted back (echoed) to the sending terminal without program intervention. The characters are also loaded into the silo. It is primarily intended for computer controlled high speed systems as a means of confirming successful reception.

If the receiver scanner finds a received character for a line which has auto-echo enabled, it examines the framing error and overrun error flags associated with that character. If either error is present, the character and associated error flag are loaded into the silo so that the system can be alerted when the NRC register is read.

The received character is auto-echoed providing three conditions are met:

a. No bus request is in progress.

b. Thc transmitter scanner is operating.

c. Space is available in the transmitter Holding Register.

Table 4-5
States of Status Flip-Flops E10 and E18

Condition Sampled	Status	Associated Flip-Flop		
		Desig	State	Output
UART Overrun	Overrun	E18–D0	Set	R0(1) High
	No Overrun		Reset	R0(1) Low
Auto-Echo	Enabled	E18–D1	Reset	R1(0) High
	Not Enabled		Set	R1(0) Low
Transmitter Scanner	Operating	E18–D2	Set	R2(1) High R2(0) Low
	Stopped		Reset	R2(1) Low R2(0) High
UART Transmitter Holding Register	Full	E18–D3	Set	R3(1) High R3(0) Low
	Empty		Reset	R3(1) Low R3(0) High
Bus Request	Requesting	E10–D0	Set	R0(1) High R0(0) Low
	Not Requesting		Reset	R0(1) Low R0(0) High
UART Framing Error	Framing Error	E10–D2	Set	R2(1) High
	No Framing Error		Reset	R2(1) Low

4.8.4.3 Normal Auto-Echo Operation – During normal auto-echo operation, the following conditions exist. Assume that SAMPLE STATUS H is asserted and sample status flip-flops E10 and E18 have been clocked (drawing D-CS-M7289-0-1, sheet 3).

a. The auto-echo enabled flip-flop for the selected line is set. Signal AE ENAB XX H is asserted and flip-flop E18–D1 is reset.

b. No bus request is in process. Signal REQUEST BUS (1) H is low and flip-flop E10–D0 is reset.

c. The transmitter scanner is operating. Signal XMIT STATUS L is high and flip-flop E18–D2 is set.

d. Space is available in the UART transmitter Holding Register for the selected line. TMBT LINE XX H is asserted and flip-flop E18–D3 is reset.

Conditions a, b, and c qualify NAND gate E6 by putting high signals on pins 1, 2, and 3. The output (pin 12) of E6 goes low, is inverted by E5, and applied to one input each of two 2-input NAND gates: E14 pin 4 and E14 pin 2. Condition d puts a high on E14 pin 1. The output (pin 3) of this gate goes low, is inverted by E2 pin 3, and puts a high on E2 pin 4. The other input of this gate (pin 5) goes high when DETERMINE NEXT H is asserted. This drives its output (pin 6) low which generates AE GO L. DETERMINE NEXT H is also sent to two other E2 gates: E2 pin 12 and E2 pin 20. Gate E2 pin 9 is high because conditions a, b, c, and d drove E6 pin 8 high. The resulting low at E2 pin 8 is sent to E1 pin 12 to qualify this gate for assertion when LOAD UART AND/OR SILO L is generated by the sequencer.

Conditions a, b, c, and d disable E6 pin 6 which in turn disables E2 pin 11 to inhibit signal ABANDON L during a normal auto-echo operation.

When asserted, AE GO L performs the following functions.

a. AE GO L is sent to the transmitter scanner logic (drawing D-CS-M7277-0-1, sheet 4) to stop the scanner.

b. AE GO L is sent to multiplexers E39 and E42 that select either the output of the byte control logic or the 8 received data bits from the UART cards (drawing D-CS-M7277-0-1, sheet 3). In this case, with AE GO L asserted, the 8 received data bits are selected. They represent the character to be echoed. These bits become TRAN DATA 1 – TRAN DATA 8 at the multiplexer output. They are sent to the transmitter data bus on the UART cards and hence to the input of the transmitter Holding Register of each UART. Subsequently, these bits will be loaded into the transmitter Holding Register of the UART that is receiving the character to be echoed. This action is provided by the AE STROBE signal and is explained below.

c. AE GO L is sent to the select (S0) input of multiplexer E34 (D-CS-M7289-0-1, sheet 3). Signal AE GO L determines whether the TRAN SCAN A, B, C, D leads are controlled by the transmitter scanner (normal case) or the receiver scanner (auto-echo case). In this case, with AE GO L asserted, the receiver scanner lines are selected. These lines are the four buffered outputs of receiver scanner counter E25 which are RECV SCAN A, B, C, and D. These bits become TRAN SCAN A, B, C, and D. These signals are sent to the DS line multiplexer (E6) on each UART card to select the Data Strobe signal (BUF DS LINE X) which loads the transmitter Holding Register. The TRAN SCAN lines are a function of the RECV SCAN lines so they point to the same UART that is receiving the character to be echoed. The loading operation does not occur until multiplexer E6 is enabled by TRAN STROBE H.

When LOAD UART AND/OR SILO L is asserted, AE STROBE H is asserted at E1 pin 4. It is sent to the M7278 module, double inverted by E47 pin 13 and E39 pin 2, and sent as TRAN STROBE H to the UART cards to enable the DS line multiplexer E6. The selected BUF DS LINE X signal is thus generated and it loads TRAN DATA 1 through TRAN DATA 8 into the transmitter Holding Register of the UART that received the character to be echoed. The received character is thus transmitted back to the sending terminal.

Signal LOAD UART AND/OR SILO L also generates a high at E1 pin 13 that is sent to the RDA decoder (E12) on the UART card which sends a BUF RDA LINE X signal to the reset data available input of the selected UART. This signal resets the UART Received Data Available flag (BUF DA LINE X).

Signal RESET DATA AVAIL, which is high, is inverted by E1 pin 10 to generated LOAD SILO L. This signal is sent to the silo control logic to initiate a load operation that places the received characters and status information into the silo.

4.8.4.4 Use of ABANDON Signal to Prevent Auto-Echo Operation – Even if auto-echo is enabled, assertion of ABANDON L can halt the auto-echo procedure if any one of three conditions is not satisfied. The conditions that can halt auto-echo are:

a. A bus request is in process. Signal REQUEST BUS (1) H is asserted which causes flip-flop E10–D0 to be set when clocked by SAMPLE STATUS H.

b. The transmitter scanner is stopped. Signal XMIT STATUS L is asserted which causes flip-flop E18–D2 to be reset when clocked by SAMPLE STATUS H.

c. The UART transmitter Holding Register is full. Signal TMBT LINE XX H is low. This causes flip-flop E18–D3 to be set when clocked by SAMPLE STATUS H.

Assume that a bus request is in process. Flip-flop E10–D0 is set and its R0(1) output is high. This signal is sent to E14 pin 12 whose other input (pin 13) is high because auto-echo is enabled. The output (pin 11) of E14 goes low and is sent to E6 pin 4. This produces a high at E6 pin 6 that is sent to E2 pin 13. When DETERMINE NEXT H is asserted, the other input (pin 12) of E2 is high and its output (pin 11) goes low. This signal is ABANDON L. It is sent to E13 pin 12 (drawing D-CS-M7289-0-1, sheet 4) which drives the output (pin 11) of this gate low, which in turn disables E43. This action allows the next 2.5 MHz clock pulse to disable the sequencer, clear RECV DATA EN (1) H, and set the RESTA SCAN flip-flop. Auto-echo operation is halted and the receiver scanner resumes operation.

If the transmitter scanner is stopped, the same result occurs except that it is initiated by a low signal at E6 pin 5. If the transmitter Holding Register is full, the same result occurs except that it is initiated by a low signal at pin 3.

4.9 FIFO BUFFER

4.9.1 Introduction

The FIFO buffer and associated control logic is located on the M7279 FIFO Buffer Module (drawing D-CS-M7279-0-1, sheets 2 and 3). This discussion is divided into four major parts:

a. Functional description of the FIFO

b. Operation of the FIFO input logic

c. Loading the FIFO

d. Reading the FIFO.

4.9.2 FIFO Buffer Functional Description

The first-in/first-out (FIFO) buffer is commonly referred to as the silo. It is a serial memory device that allows the first data entered to be the first data removed, regardless of the quantity of data stored.

The FIFO buffer or silo is composed of four type 3341 64-word by 4-bit FIFO serial memory devices E3, E8, E13, and E17 (drawing D-CS-M7279-0-1, sheet 3). The four 3341s are connected to provide a buffer that is 16-bits wide and 64-words deep. All four devices use common load and unload control signals. The Ready In flags of all 3341s are ANDed to provide READY IN L at E9 pin 6. All the Ready Out flags are ANDed to provide READY OUT L at E9 pin 8.

Actually only 15 silo bits are used. They are identified as NRC 00 H – NRC 14 H and, together with NRC 15 H from the silo control logic, they constitute the Next Received Character (NRC) Register. Except for bit 15, the NRC register is the silo output. Table 4-6 identifies the NRC bits.

Table 4-6
NRC Bit Identification

Input	Output	Remarks
RCV DATA 01 H	NRC 00 H	
RCV DATA 02 H	NRC 01 H	From FIFO E3
RCV DATA 03 H	NRC 02 H	
RCV DATA 04 H	NRC 03 H	
RCV DATA 05 H	NRC 04 H	
RCV DATA 06 H	NRC 05 H	From FIFO E8
RCV DATA 07 H	NRC 06 H	
RCV DATA 08 H	NRC 07 H	
RCV SCAN A H	NRC 08 H	
RCV SCAN B H	NRC 09 H	From FIFO E17
RCV SCAN C H	NRC 10 H	
RCV SCAN D H	NRC 11 H	
MASTER PE H	NRC 12 H	From FIFO E13
MASTER FE H	NRC 13 H	
MASTER OR H	NRC 14 H	
–	NRC 15 H	From NRC 15 H Flip-Flop

High signals are used to load and unload the silo. Simultaneous loading and unloading of the silo is prevented by the control logic.

4.9.3 FIFO Input Logic

The inputs to the silo are obtained from four type 74157 quad 2-line to 1-line multiplexers. Each multiplexer (E2, E7, E12, and E16) chooses between two 4-bit input words (drawing D-CS-M7279-0-1, sheet 2). The A word contains data. The B word contains a fixed binary representation that is obtained by connecting the B0 and B3 inputs to ground and connecting the B1 and B2 inputs to +3 V. If the B word is selected by the input multiplexers, the NRC even-numbered bits (00, 02, 04, etc.) are forced to 0 and the NRC odd-numbered bits (01, 03, 05, etc) are forced to 1.

The input word selection is controlled by signal SSR 15 H that is connected to the select (S0) input of each multiplexer. Signal SSR 15 H is the maintenance bit in the Silo Status Register (SSR). During normal operation it is low and the A word or data word is selected. When it is desired to check the silo for maintenance purposes, the program sets bit 15 of the SSR. Signal SSR 15 H goes high and the B word or fixed test pattern is selected.

Multiplexers E2 and E7 provide the eight received data bits (RCV DATA 01 H – RCV DATA 08 H). The inputs to these multiplexers come from the received data bus on the UART cards. Corresponding bits from each card (UC1 and UC2) are ORed and sent to the appropriate A word input.

Multiplexer E16 provides the receiver scanner signals (RCV SCAN A, B, C, and D). The inputs to the multiplexer come from the output of the receiver scanner counter (E25) on the M7289 module.

Multiplexer E12 provides the Parity Error flag (MASTER PE H), the Framing Error flag (MASTER FE H), and the Overrun Error flag (MASTER OR H). The inputs to E12 come from decoders on the UART cards that send the status of these flags for the received character. Corresponding flag signals from each UART card (UC1 and UC2) are ORed and sent to the appropriate A word input.

4.9.4 Loading the FIFO (SILO)

A silo loading operation is initiated by the receiver scanner when it asserts LOAD SILO L. This signal is inverted by E15 pin 2 and clocks the LOAD REQ flip-flop. This redefined flip-flop has its D input permanently connected to ground so it is set by the clock pulse. The (1) H output of LOAD REQ is high and is sent to the D input of the LOAD flip-flop. This flip-flop and the UNLOAD flip-flop are both clocked by the outputs of the PHASE flip-flop. Simultaneous loading and unloading of the silo is possible but not allowed. It is prevented by connecting the PHASE flip-flop in a toggle configuration and clocking the LOAD and UNLOAD flip-flops with the complementary outputs of the PHASE flip-flop (Figure 4-27). The LOAD flip-flop is clocked when the PHASE flip-flop goes to the 0 state and the UNLOAD flip-flop is clocked when the PHASE flip-flop goes to the 1 state.

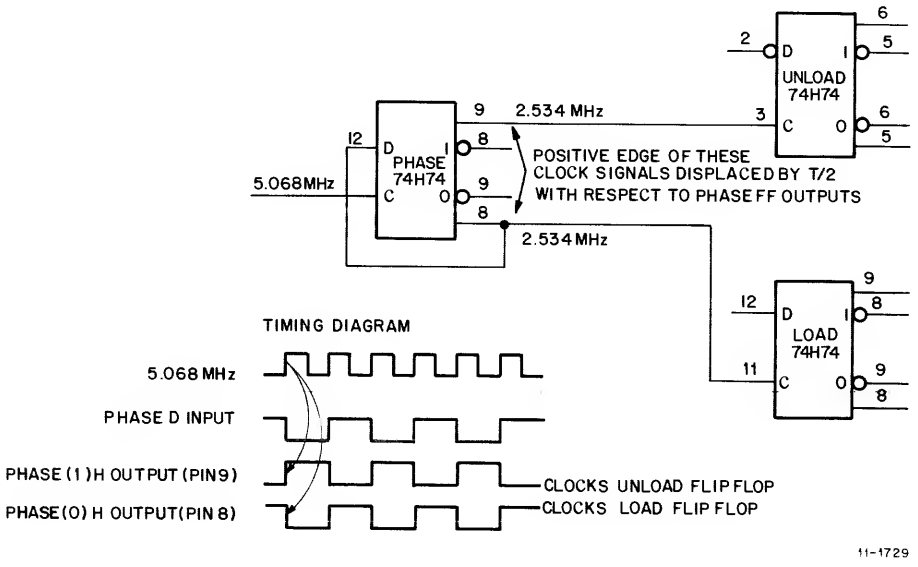


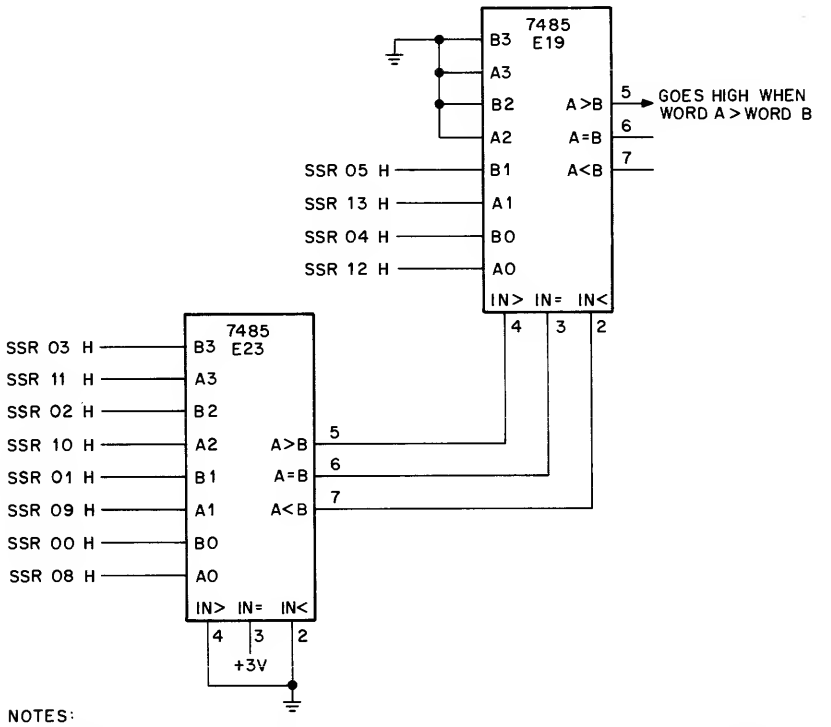
Figure 4-27 Generation of Clock Pulses for LOAD and UNLOAD Flip-Flops

In this case, with the D input of the LOAD flip-flop high, the next time the PHASE flip-flop goes to the 0 state, the LOAD flip-flop is clocked which sets it. The (1) L output of LOAD, which is low, triggers the LOAD STROBE one-shot. A 170 ns positive pulse is generated at the (1) H output (pin 6) of LOAD STROBE which is sent to the load input (pin 3) of the silo.

At the end of the 170 ns pulse, the (0) H output (pin 1) of LOAD STROBE comes high again. This signal is sent to a delay network (E4, DL1, and E14) that generates a 30 ns negative pulse at E14 pin 11 called LOAD PULSE L. This signal restarts the receiver scanner. The positive trailing edge of LOAD PULSE L also increments the silo level counter that is composed of two cascaded type 74193 synchronous counters (E24 and E20). LOAD PULSE L is also double inverted by E15 pin 4 and E26 pin 4 to clear the LOAD REQ flip-flop. This is the end of the load cycle.

The six binary outputs of the silo level counter (E20 and E24) represent the number of characters in the silo. They constitute bits 08 – 13 of the Silo Status Register (SSR) and can be read by the program. Six binary bits give 64 counts ($2^6 = 64$); however, the states of these bits indicate 0 through 63_{10}. A full silo contains 64 characters and is represented as 000000. An empty silo is represented as 000000 also. The program can tell the difference by reading SCR 14 which is high when the silo is full and is the storage interrupt bit.

The silo level counter outputs go to two type 7485 4-bit magnitude comparators (Figure 4-28). They are cascaded to provide comparison of two 6-bit words. The counter outputs are the A input word, and SSR bits 00–05 and the B input word. SSR 00–SSR 05 are the silo alarm level bits. They are program selectable to determine at what silo fill level a receiver interrupt is to be requested. When the number of characters in the silo exceeds the silo alarm level, an interrupt is requested provided the receiver interrupt enable bit in the System Control Register (SCR 06) is set.



NOTES:
1. When cascaded, the 7485 handling the least significant bits must be permanently connected as shown.
2. Word A consists of bits SSR 08 H - SSR 13 H which represent the number of characters in the silo as indicated by the silo character counter (E20 and E24).
3. Word B consists of bits SSR 00 H - SSR 05 H which represent the silo alarm level (0, 1, 2, 4, 8, 16 or 32) as determined by the program.

11-1728

Figure 4-28 Silo Fill/Alarm Level Comparator

In the silo control logic, when the number of bits in the silo (A word) exceeds the silo alarm level (B word), output A > B of E19 goes high. This signal is sent to E14 pin 1. Assume that a character is available at the silo output. READY OUT L is asserted at E9 pin 8, is inverted by E22 pin 8, and is sent to E14 pin 2. The output (pin 3) of E14 goes low, is inverted by E22 pin 2, and clocks the DATA READY flip-flop. This redefined flip-flop is set and its (1) L output (pin 5) is low, which is DATA READY L. This signal is sent to the SCR output logic on module M7289 to initiate a receiver interrupt.

4.9.5 Reading the FIFO (SILO)

Assume that the program desires to read the NRC register in response to the DATA READY flag.

When the NRC register is addressed, signal READ NRC H is asserted by the M7277 module. When READ NRC H goes high, it clocks the NRC 15 flip-flop. A character is available at the silo output so READY OUT L is asserted at E9 pin 8. This puts a low on the D input of the NRC 15 flip-flops. When clocked by READ NRC H, this redefined flip-flop is set. This means that when the instruction to read the NRC register is issued, valid data is available because READY OUT L is asserted.

Signal NRC 15 H is asserted at the (1) H output (pin 8) of the NRC 15 flip-flop. NRC 15 H is inverted by E26 pin 10 to clear the DATA READY flip-flop. This clears the Data Ready flag (DATA READY L). NRC 15 H also puts a high on E14 pin 5. The other input (pin 4) of this gate remains low until READ NRC H goes low again after the NRC register has been read. Then pin 4 is high and E14 pin 6 goes low and is sent to the D input of the UNLOAD flip-flop. The next time that the PHASE flip-flop goes to the 1 state, its (1) H output clocks the UNLOAD flip-flop which sets it. The (1) L output (pin 5) of the UNLOAD flip-flop triggers the UNLOAD STROBE one-shot. The (1) H output (pin 6) of UNLOAD STROBE provides a 100 ns positive pulse that is sent to the unload input (pin 15) of the silo. This action shifts out the NRC character that has just been read and lets the next character fall into the last position in the silo.

At the end of the 100 ns pulse, the (0) H output (pin 1) of UNLOAD STROBE comes high again. This signal is sent to a delay network (E4, DL2, and E14) that generates a 30 ns negative pulse at E14 pin 8. The positive trailing edge of this signal decrements the silo level counter. This signal is also double inverted by E22 pin 4 and E26 pin 13 to clear the NRC flip-flop.

If there is another character in the silo, the action of that character falling into the last position in the silo causes READY OUT L to be asserted at E9 pin 8. If the silo fill level remains in excess of the silo alarm level, E14 pin 1 is high and E14 pin 2 is high. This action sets the DATA READY flip-flop again and another receiver interrupt is generated provided the receiver interrupt enable bit (SCR 06) is set.

4.10 SYSTEM CONTROL REGISTER

4.10.1 , General Information

The System Control Register (SCR) is contained on the M7289 System Control and Receiver Scan Module (drawing M7289-0-1, sheet 6).

The SCR contains 16 bits and is byte addressable. The low byte (bits SCR 00 – SCR 07) is clocked by LOAD SCR LOW BYTE H and the high byte (bits SCR 08 – SCR 15) is clocked by LOAD SCR HIGH BYTE H.

All 16 bits are stored in D type flip-flops. Two type 74175 quad flip-flop packages are used for 8 bits; E7 for bits SCR 00 – SCR 03 and E47 for bits SCR 09 and SCR 11 – SCR 13. Four type 7474 dual flip-flop packages are used for the other 8 bits; E11 for SCR 04 and SCR 05, E19 for SCR 06 and SCR 07, E41 for SCR 08 and SCR 10, and E50 for SCR 14 and SCR 15.

The D input to each flip-flop comes from a correspondingly numbered Unibus data line whose signal has passed through a Unibus receiver and noninverting buffer on module M7278. Each bit is under program control but several bits are also under DH11 hardware control. In addition, the SCR contains logic that allows interaction between various SCR bits and the DH11 hardware. The interaction is primarily with respect to the generation of interrupts. Only SCR outputs SCR 00 H – SCR 05 H and SCR 11 H are used directly without interaction with other SCR bits.

Outputs SCR 00 H – SCR 03 H are the line selection bits. They are sent to the control strobe logic (drawing D-CS-M7277-0-1, sheet 3) to generate the LPR clock signals. These bits are also sent to the CAR (drawing D-CS-M7277-0-1, sheet 6) as the address selection bits for the CA memory.

Outputs SCR 04 H and SCR 05 H are sent to the CAR (drawing D-CS-M7277-0-1, sheet 5) as bits 16 and 17 of the current address.

Output SCR 11 H is sent to the address selection logic (drawing D-CS-7277-0-1, sheet 3) to generate an initialize signal within the DH11.

The remainder of the SCR outputs are interactive and are discussed with respect to the functions that they perform; primarily, the generation of receiver and transmitter interrupts.

4.10.2 Receiver Interrupt Bits

Bits SCR 06, SCR 07, SCR 12, and SCR 14 are related to the generation of a receiver interrupt. For clarity, a simplified logic diagram (Figure 4-29) is used to show only these bits and associated logic.

In normal operation, the maintenance bit (SCR 09) is cleared by the program and SCR 09 H is low. This signal is sent to the pin 5 input of two type 74121 one-shots; SCR 07 LOAD (E23) and SCR 10 LOAD (E25). A low on this input inhibits the operation of the one-shot. As a result, the SCR 07 flip-flop and SCR 14 flip-flop cannot be clocked when their respective load signals are generated. These signals are LOAD SCR LOW BYTE H for SCR 07 and LOAD SCR HIGH BYTE H for SCR 14.

There are two kinds of receiver interrupts. One is generated when the program has set the receiver interrupt enable bit (SCR 06) and a character is available in the silo. The other is generated when the program has set the storage interrupt enable bit (SCR 12) and the silo is full at the time that the DH11 needs to store an additional character there.

Assume that the receiver interrupt enable bit (SCR 06) is set. This is accomplished by the program as follows. BUF DATA 06 H is asserted at the D input of the SCR 06 flip-flop. The processor addresses the SCR register with an instruction to write into the low byte. The address selection logic generates LOAD SCR LOW BYTE H which clocks the SCR 06 flip-flop and its (1) H output (pin 9) goes high. This signal is sent to E31 pin 9. Assume that the SCR 07 flip-flop is cleared. If this flip-flop is not cleared, the act of DATA READY L going low does not produce the transition of RCV INT REQ H needed to cause the M7821 to start an interrupt sequence. Its (1) L output (pin 6) is high and is sent to E31 pin 12. When the number of characters exceeds the silo level limit, DATA READY L is asserted by the silo logic to indicate that a character is available. DATA READY L is sent to E31 pin 13 and the output (pin 11) of this gate goes high and is sent to E31 pin 10. The output of this gate (pin 8) goes low and is inverted by E31 pin 5 to generate RCV INT REQ H. This signal is sent to the M7821 module in slot A06 to initiate the receiver interrupt sequence.

Assume that the storage interrupt enable bit (SCR 12) has been set by the program. This produces a high at output R3 (1) of flip-flop E47 that is sent to E31 pin 1. When the receiver scanner has found a character to be stored but the silo is full, STORAGE OVERFLOW L is asserted and sent to the preset input (pin 10) of the SCR 14 flip-flop which sets it. The (1) H output (pin 9) of the SCR 14 flip-flop is high. It is sent to E31 pin 2 and the output (pin 3) of this gate goes low. This signal is inverted by E31 pin 4 to generate RCV INT REQ H.

4.10.3 Transmitter Interrupt Bits

Bits SCR 10, SCR 13, and SCR 15 are related to the generation of a transmitter interrupt. For clarity, a simplified logic diagram (Figure 4-30) is used to show only these bits and related logic.

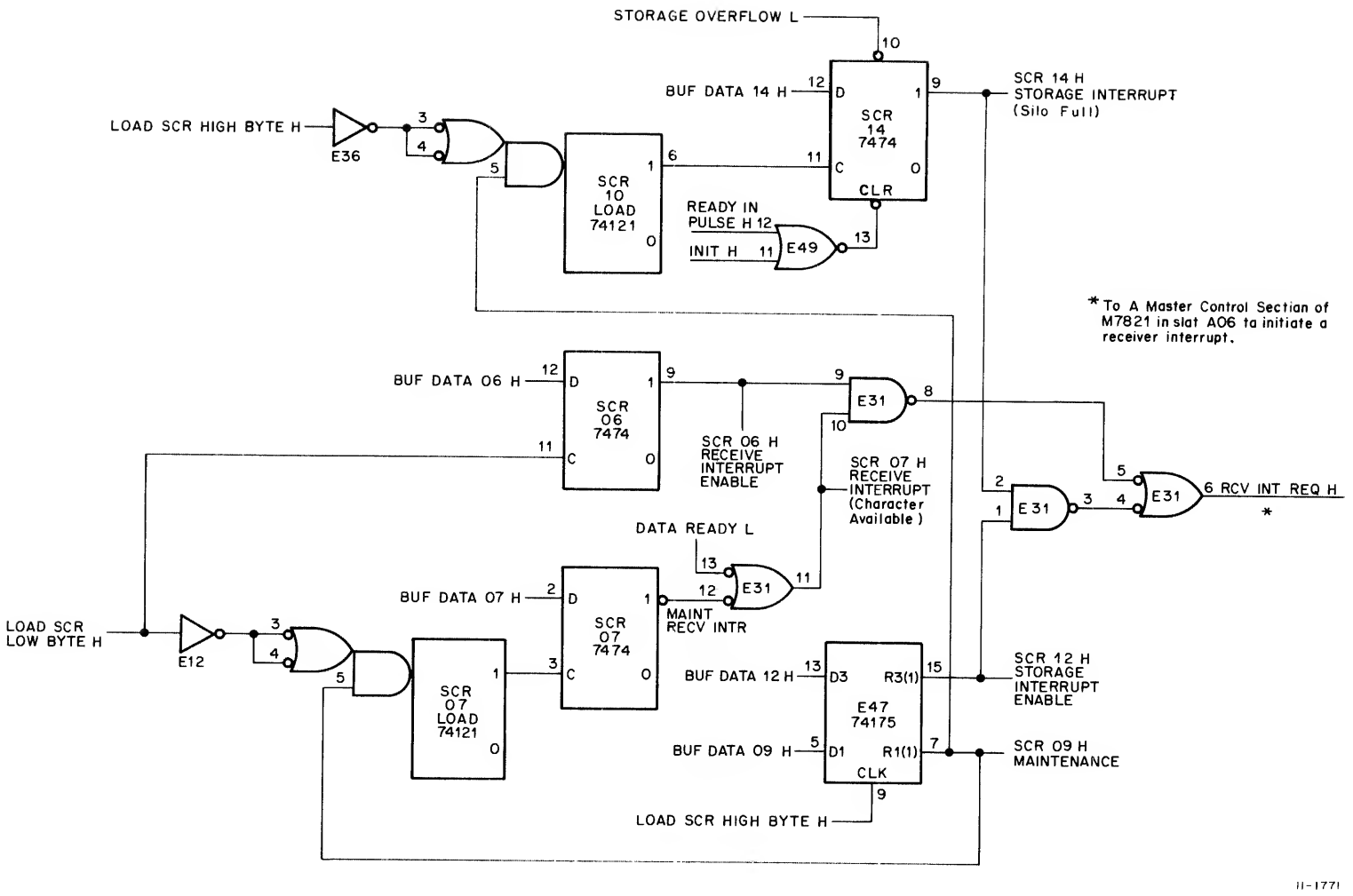


Figure 4-29 Simplified Logic Diagram of SCR Receiver Interrupt Circuitry

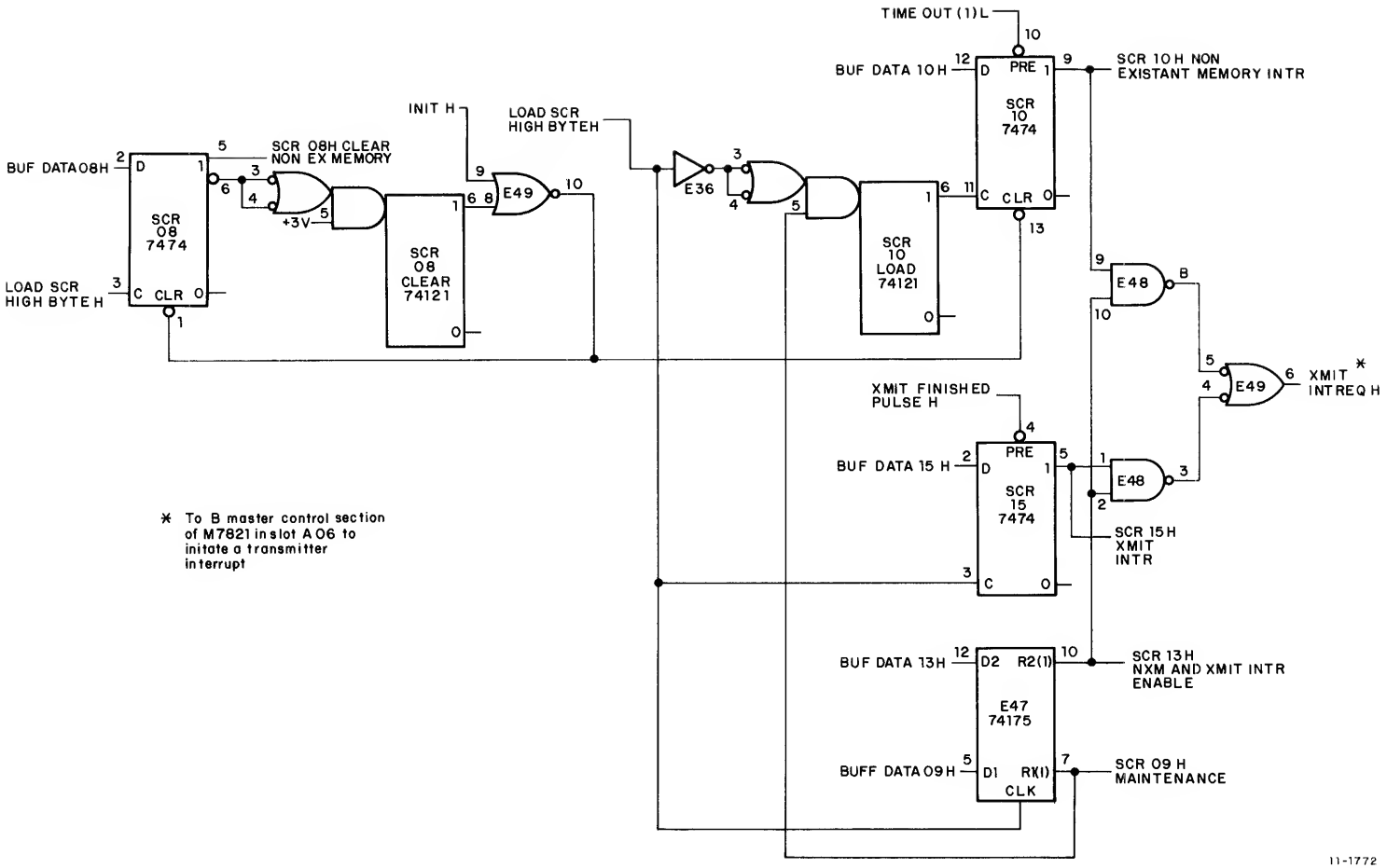


Figure 4-30 Simplified Logic Diagram of SCR Transmitter Interrupt Circuitry

In normal operation, the maintenance bit (SCR 09) is cleared by the program and SCR 09 H is low. This signal inhibits the operation of the SCR 10 LOAD one-shot. As a result, the SCR 10 flip-flop cannot be clocked when LOAD SCR HIGH BYTE H is asserted.

There are two kinds of transmitter interrupts and their generation is dependent on the transmitter and nonexistent memory interrupt enable bit (SCR 13) being set by the program. One interrupt is generated when one or more lines has finished transmission. The other interrupt is generated when the DH11 addresses nonexistent memory.

Assume that the transmitter interrupt enable bit (SCR 13) is set. Signal SCR 13 H, which is high, is sent to one input each of two E48 NAND gates. At the end of the NPR cycle that loads the last character to be transmitted, the Byte Count Register overflows (goes to 0) and this event generates signal XMIT FINISHED PULSE L. This low signal is sent to the preset (pin 4) input of the SCR 15 flip-flop which sets it. The (1) H output (pin 5) of the SCR 15 flip-flop goes high. It is sent to E48 pin 1 which drives the output (pin 3) of this gate low. This signal is inverted by E48 pin 6 to generate XMIT INT REQ H. This signal is sent to the M7821 module in slot A06 to initiate the transmitter interrupt sequence.

Assume now that the DH11 is performing a DATI transaction but the CAR places a nonexistent memory address on the Unibus. Because it is an erroneous address, no SSYN response is generated and, after 20 μs, the TIME OUT flip-flop on the M796 Unibus Master Control Module is set. The DATI transaction is discontinued. Signal TIME OUT (1) L is asserted by the M796 module and sent to the preset (pin 10) input of the SCR 10 flip-flop which sets it. The (1) H output (pin 9) goes high and is sent to E48 pin 9. The other input (pin 10) of this gate is also high because the transmitter interrupt enable bit (SCR 13) is set; therefore, the output (pin 8) goes low. This signal is inverted by E48 pin 6 to generate XMIT INT REQ H.

During normal operation, the SCR 10 flip-flop is read-only. Once set, it can be cleared only by the program via bit SCR 08. The program sets flip-flop SCR 08 and its (1) L output, which is low, is sent to the input of one-shot SCR 08 CLEAR. This signal triggers the one-shot and a 40 ns positive pulse from its (1) H output (pin 6) is inverted by E49 pin 10 and sent to the clear input (pin 13) of flip-flop SCR 10 which clears it. This signal also directly clears the SCR 08 flip-flop and the TIME OUT flip-flop on the M796 module.

4.10.4 Maintenance Mode

In the maintenance mode, the program can generate the receiver and transmitter interrupt request signals. The program selects the maintenance mode by setting the maintenance bit (SCR 09). Signal SCR 09 H is sent to input pin 5 of one-shots SCR 07 LOAD and SCR 10 LOAD which qualifies them. Now, if the program desires to generate a receiver interrupt request signal, it sets Unibus data bits D06 and D07. When LOAD SCR LOW BYTE H is asserted, it clocks the SCR 06 flip-flop and sets it. This load signal is inverted by E12 pin 6 which triggers one-shot SCR 07. The positive pulse from this one-shot clocks the SCR 07 flip-flop and sets it. The (1) L output from the SCR 07 flip-flop is inverted by E31 pin 11 and puts a high on E31 pin 10. The other input of this gate (pin 9) is high also because the SCR 06 flip-flop is set. The output (pin 8) of E31 goes low and is inverted by E31 pin 6 to generate RCV INT REQ H.

If the program desires to generate a transmitter interrupt request signal, it sets Unibus data bits D13 and D10 or D13 and D15. The generation of the transmitter interrupt request signal XMIT INT REQ H occurs in the same way as that described in Paragraph 4.10.3 except that flip-flops SCR 10 and SCR 14 are clocked via one-shot SCR 10 LOAD under program control rather than being directly set by the hardware.

4.11 HALF/FULL DUPLEX CONTROL LOGIC

The logic for controlling half/full duplex operation is contained on the M7289 System Control and Receiver Scan Module (drawing D-CS-M7289-0-1, sheet 5). Logic is also provided to allow local looping of a transmitted character for maintenance purposes.

The logic consists of four type 74157 quad 2-line to 1-line multiplexers and three gates for each of the 16 lines. Figure 4-31 shows the logic for line 07 which is typical of all lines. Multiplexer E27 chooses between two 4-bit input words labeled A and B. The B word is SERIAL OUT LINE 07 which is the transmitted character from the UART. This word is selected during the maintenance mode. The A word is the output of the half/full duplex control logic. This word is selected during normal operation and can be TTL DATA IN 07 or it can indicate a break condition.

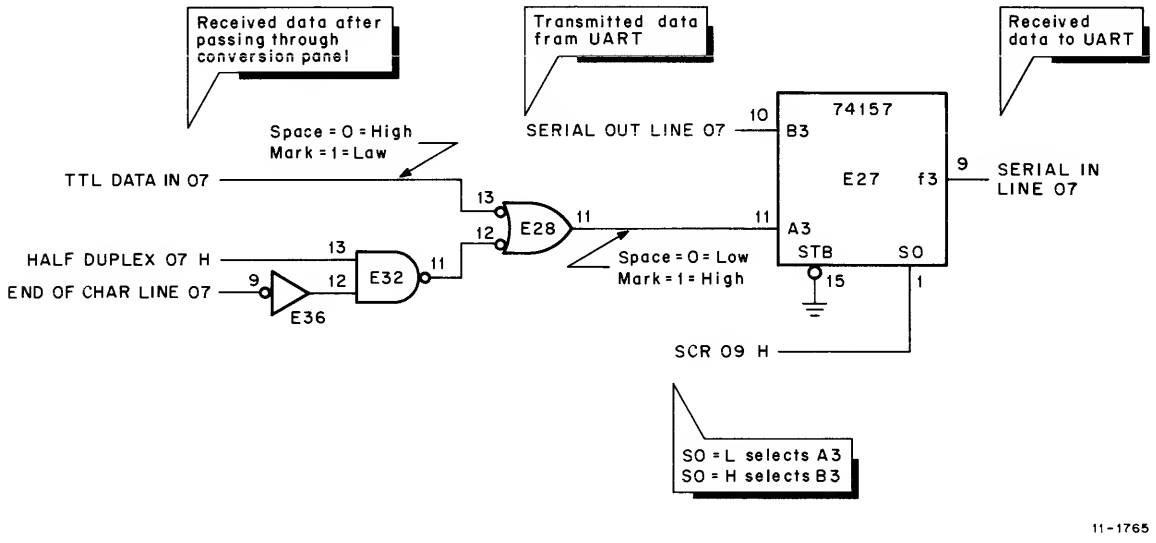


Figure 4-31 Typical Half/Full Duplex Line Control Logic

Word selection is provided by signal SCR 09 H which is sent to the selected (S0) input of multiplexer E27. SCR 09 is the maintenance bit of the System Control Register. When it is high, the DH11 is placed in the maintenance mode and input word B is selected. When SCR 09 H is low, the DH11 is placed in the normal operating mode and input word A is selected.

Assume that the maintenance mode (word B) is selected. A transmitted character is sent serially from UART number 7 as SERIAL OUT LINE 07 to the B3 input of multiplexer E27. It is enabled to the output (f3) of E27 as SERIAL IN LINE 07 which is sent to the receiver input of UART number 7. In this mode, a character can be looped back to check portions of the DH11 for maintenance purposes.

In the normal operating mode, SCR 09 H is low and word A is selected. If the system is to be operated in the full duplex mode, the program clears LPR bit 14 which makes HALF DUPLEX 07 H low. This drives the output (pin 11) of E32 high which in turn is sent to pin 12 of E28. The other input (pin 13) of E28 is TTL DATA IN 07 which is received data that has passed through the level conversion/distribution panel. During conversion, the received data is inverted; however, it is restored by another inversion as it passes through E28.

From the output (pin 11) of E28, it enters input A3 of multiplexer E27 and leaves via output f3 as SERIAL IN LINE 07. This line is connected to the serial data input of the receiver in UART number 7.

If the system is to be operated in the half duplex mode, the receiver for line 07 must be blinded when the transmitter for line 07 is sending a character. In the half duplex system, the output data from both terminals is ORed and presented to both terminal receivers. The sending terminal receives its own transmission. In the DH11, this is prevented by blinding the UART receiver so that it does not receive its own transmission (Figure 4-32). In this way, the computer does not process its own transmission as received data.

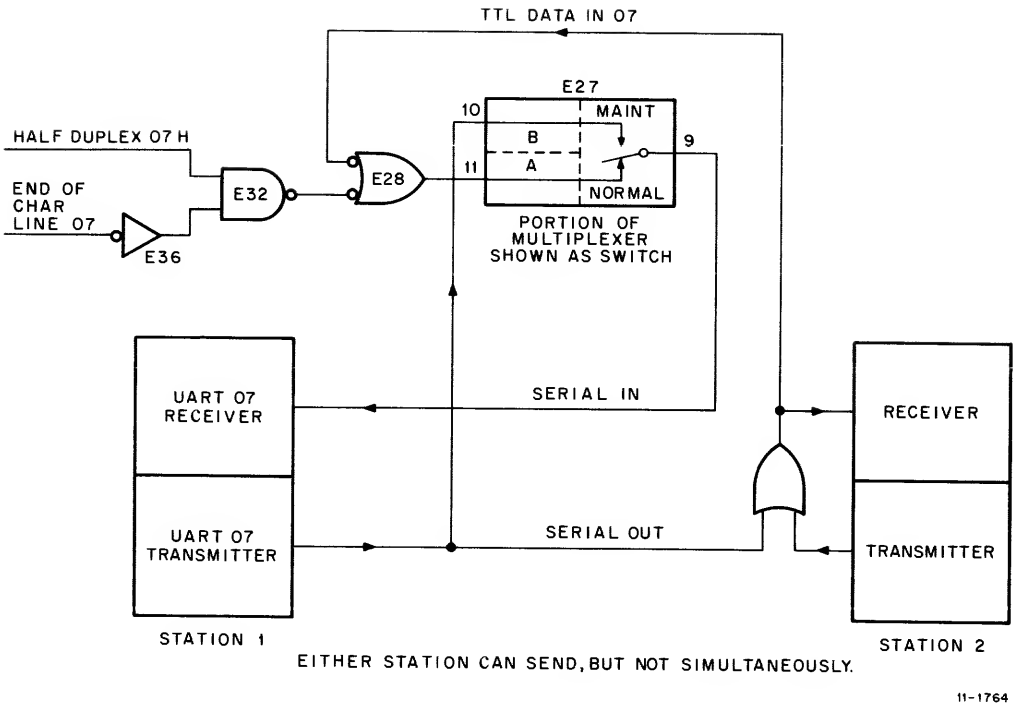


Figure 4-32 Half Duplex Connection and Maintenance Logic

Operation in the half duplex mode requires that HALF DUPLEX 07 H be asserted. This puts a high on E32 pin 13. The other input (pin 12) is the inversion of END OF CHAR LINE 07. This signal comes from the UART and goes low whenever a character is being transmitted on this line. When UART transmitter 07 is sending a character, END OF CHAR LINE 07 is low. It is inverted by E36 and puts a high on E32 pin 12. The output (pin 11) of E32 goes low and is sent to E28 pin 12. With this pin held low, the output of E28 remains high regardless of the state of the other input which is TTL DATA IN 07. This high signal, which represents an idle line condition, is sent to UART receiver 07 and blinds it.

4.12 REGISTERS AND BYTE COUNT MODULE M7278

4.12.1 Introduction

The M7278 module contains the Byte Count Register (BC), Line Parameter Register (LPR), Buffer Active Register (BAR), Break Control Register (BCR), and portions of the Silo Status Register (SSR). It also contains the Unibus data line receiver and drivers and a multiplexer circuit for reading all DH11 registers. The Byte Count Register has been described previously in Paragraph 4.7.

4.12.2 Unibus Data Line Receivers and Buffers

The inputs to the registers on the M7278 module come from the Unibus data line signals D(15:00). Each Unibus signal (BUS D XX L) is sent to a type 380 Unibus receiver whose output is buffered by a type 7417 non-inverting buffer. This buffered signal (BUF DATA XX H) is sent to the appropriate input of each register. The receivers and buffers are shown in drawing D-CS-M7278-0-1, sheets 3 and 4.

4.12.3 Line Parameter Register

The Line Parameter Register (LPR) is composed of four type 74175 quad flip-flop packages as shown in Table 4-7.

Table 4-7
Line Parameter Register Components

LPR Bit	Device Desig	Location
12–15	E52	Sheet 5
8–11	E37	Sheet 6
4–7	E59	Sheet 7
0–3	E61	Sheet 8

Each 74175 contains four D-type flip-flops with complementary outputs. Signals BUF DATA 00 H through BUF DATA 15 H are sent to the D inputs. To write into the LPR, signal LOAD LPR H is generated by the address selector when the LPR address is decoded. LOAD LPR H is used to clock the LPR flip-flops. The 1 output of each bit is sent to the D2 inputs of the register read-out multiplexer. The 0 output of each bit is sent to other DH11 logic as described below.

1. Bits 00 through 05 are buffered and inverted by type 7437 NAND buffers and sent to the M7280 UART cards to select character length, number of stop bits, and parity function.

2. Bits 06 through 09 are sent to the M7288 Line Parameter Control Module to control the speed of the selected receiver.

3. Bits 10 through 13 are sent to the M7288 Line Parameter Control Module to control the speed of the selected transmitter.

4. Bits 14 and 15 are sent to the M7288 Line Parameter Control Module to control the half/full duplex and auto-echo modes.

4.12.4 Buffer Active Register

The Buffer Active Register (BAR) is composed of eight 7474 dual D-type flip-flops as shown in Table 4-8.

Table 4-8
Buffer Active Register Components

BAR Bit	Device Desig	Location
14 and 15	E55	Sheet 5
12 and 13	E54	
10 and 11	E63	
8 and 9	E62	Sheet 6
6 and 7	E70	
4 and 5	E71	Sheet 7
2 and 3	E79	
0 and 1	E78	Sheet 8

Each 7474 contains two D-type flip-flops with complementary outputs. Signals BUF DATA 00 H through BUF DATA 15 H are sent to the D inputs. To write into the BAR, signal LOAD BAR LB + HB L is generated by the address selector when the BAR address is decoded. This signal is sent to two 7437 NAND buffers, E73 pin 12 (drawing D-CS-M7278-0-1, sheet 7) and E73 pin 2 (drawing D-CS-M7278-0-1, sheet 5). The E73 gates invert and

buffer LOAD BAR LB + HB L to generate the clock signals for the BAR. These signals are LOAD BAR A H which clocks bits 00 – 07 and LOAD BAR B H which clocks bits 08 – 15. Only the (1) H output of the BAR flip-flops is used. Each output is sent to the D5 inputs of the register read-out multiplexer. These signals (BAR 00 H – BAR 15 H) are also sent to the transmitter scanner on the M7277 module.

4.12.5 Break Control Register

The Break Control Register (BCR) is composed of four 74175 quad flip-flop packages as shown in Table 4-9.

Table 4-9
Break Control Register Components

BCR Bit	Device Desig	Location
12–15	E51	Sheet 5
8–11	E38	Sheet 6
4–7	E67	Sheet 7
0–3	E60	Sheet 8

Each 74175 contains four D-type flip-flops with complementary outputs. Signals BUF DATA 00 H through BUF DATA 15 H are sent to the D inputs. To write into the BCR, signal LOAD BCR H is generated by the address selector when the BCR address is decoded. LOAD BCR H is used to clock the BCR flip-flops. The 1 output of each bit is sent to the D6 inputs of the register read-out multiplexer. The 0 output of each bit is ANDed with the serial data (SERIAL OUT LINE XX) from the UART transmitter of the correspondingly numbered line. Type 7400 2-input NAND gates are used. The output of each gate (TTL DATA OUT XX) is sent to the conversion panel. Setting a BAR bit generates a break condition at the output of the gate corresponding to that bit number.

4.12.6 Silo Status Register

Only bits 0 – 5, 14, and 15 of the Silo Status Register (SSR) are contained on the M7278 module. This portion of the SSR is implemented by three 74175 quad flip-flop packages as shown in Table 4-10.

Table 4-10
Silo Status Register Components

SSR Bit	Device Desig	Location
14 and 15	E53	Sheet 5
4 and 5	E68	Sheet 7
0–3	E69	Sheet 8

The other SSR bits are: 8 – 13 which represent the silo fill level and are located on the M7279 module; and 6 and 7 which represent current address bits A16 and A17 and are located on the M7277 module.

The SSR is byte addressable; therefore, two clocking signals are used (one for each byte). To write into the SSR, signal LOAD SSR LOW BYTE H or LOAD SSR HIGH BYTE H is generated by the address selector when the SSR address is decoded with the desired byte requested (DATOB low byte or DATOB high byte). Each bit of the SSR is sent to the D7 inputs of the register read-out multiplexer.

Bits SSR 00 H – SSR 05 H from the 1 outputs of the SSR flip-flops are sent to the silo logic on the M7279 module. When set, bit SSR 15 H triggers one-shot E77 (drawing D-CS-M7279-0-1, sheet 5) to generate SILO MAINT PULSE L. SSR 15 H is sent to the silo multiplexers (module M7279) to generate a test pattern to check the silo during maintenance. SILO MAINT PULSE L is sent to the receiver scanner (module M7289) to initiate a SILO LOAD.

4.12.7 Output Multiplexer and Unibus Drivers

When a DH11 register is read, its output is placed on the Unibus data lines via 16 type 8881 drivers that are enabled by DATA TO BUS H. This signal is generated by the address selector when a read operation (DATI) is selected.

All registers share the same 16 Unibus drivers. This is accomplished by multiplexing the outputs of the registers. Sixteen type 74151 8-line to 1-line multiplexers are used. The same numbered bit from each register is sent to one multiplexer (16 multiplexers total). The single output of each multiplexer is sent to a Unibus driver. Figure 4-19 shows the arrangement for bit 00. The desired register is selected by signals DATA SOURCE A H, DATA SOURCE B H, and DATA SOURCE C H which are buffered Unibus address line signals BUS A 01 L, BUS A 02 L, and BUS A 03 L.

The read output multiplexers are located on the following sheets of the D-CS-M7278-0-1 drawing.

Sheet 5: E35, E28, E20, and E12
Sheet 6: E13, E21, E29, and E36
Sheet 7: E66, E58, E50, and E44
Sheet 8: E65, E57, E49, and E43

4.13 M7280 MULTIPLE UART CARD

The M7280 card is a quad-size module that contains eight UARTs and associated decoding, multiplexing, and gating logic for specific control and flag signals. It also contains a −12 V supply composed of discrete components operating on a −15 V source. Refer to Appendix D for a description of the UART.

Figure 4-33 shows the logic for decoding and multiplexing selected signals. Only one UART is shown but it is typical of all eight UARTs on the card.

4.13.1 Transmitter Input Data and Data Strobe Signal

The data to be transmitted (TRAN DATA 1–8) is sent in parallel to 7408 buffers and then to all UARTs as BUF TRAN DATA 1–8. The data is used only by the selected UART when its Data Strobe signal (BUF DS LINE X) goes high to place the data in the transmitter Data Holding Register.

The Data Strobe signal for a particular UART is selected by external logic. These external signals are used to control a multiplexer (E6) so that the Data Strobe signal for any one of the eight UARTs can be selected. For the DH11, the transmitter scanner logic selects the appropriate Data Strobe signal. E6 is a 74155 dual 2-line to 4-line multiplexer that is connected as a 3-line to 8-line decoder (Paragraph 4.8.2).

4.13.2 Receiver Output Data and Received Data Enable Signal

The parallel received data outputs (BUF RCV DATA 1–8) from all UARTs are wire-ORed to form a bus. Only data from the selected UART is placed on the bus when its Received Data Enable signal (BUF RDE LINE X) goes low. The bus data is inverted and sent as RCV DATA 1–8 to external logic for processing. In the DH11, these data bits go to the FIFO logic. The received Data Enable signal for a particular UART is selected by external logic. These external signals are used to control a multiplexer (E9) so that the Received Data Enable signal for any one of the eight UARTs can be selected. For the DH11, the receiver scanner logic (Paragraph 4.8) selects the appropriate Received Data Enable signal. E9 is a 74155 multiplexer that operates identically to E6 described in Paragraph 4.13.1.

4.13.3 Reset Data Available Signal

The Reset Data Available signal (BUF RDA LINE X) is driven low to reset the Received Data Available line after the external logic has accepted the received data from the selected UART. Multiplexer E12 is used to select the proper Reset Data Available Signal as a function of external logic. For the DH11, it is the receiver scanner logic. E12 is a 74155 multiplexer that operates identically to E6 described in Paragraph 4.13.1.

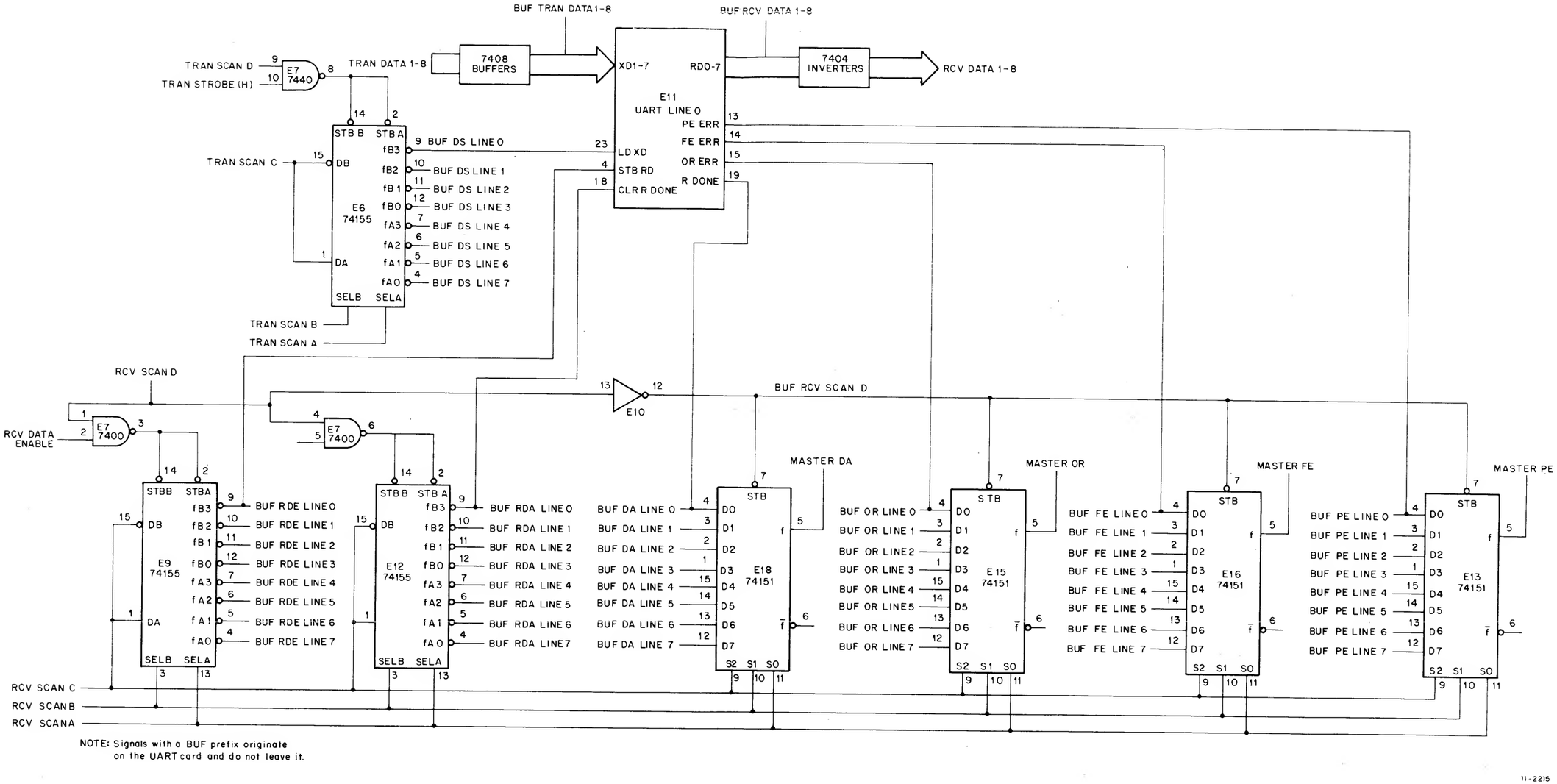


Figure 4-33 Block Diagram of Single UART Showing Decoding of Control Signals and Multiplexing of Flag Signals

4.13.4 Status Signals

Four UART status signals are sampled and sent to external logic.

a. Received Data Available (BUF DA LINE X), which goes high when a complete character has been transferred to the receiver Data Holding Register.

b. Overrun (BUF OR LINE X), which goes high if the previously received character is not read before the present character is transferred to the receiver Data Holding Register.

c. Framing Error (BUF FE LINE X), which goes high if the received character has no valid stop bit.

d. Receive Parity Error (BUF PE LINE X), which goes high if the received character parity does not agree with the selected parity.

Each status signal is handled in the same way. The Overrun signal is discussed as a typical example. The Overrun signal from each UART is sent to the input of a 74151 data selector (E15). External signals are used to control the data selector. For the DH11, the receiver scanner logic selects the appropriate Overrun signal. The data selector picks one of eight Overrun signals and sends it to the external logic as MASTER OR. Sixteen UARTs (two UART cards) are used in the DH11 so that the MASTER OR signals from both cards are ORed to provide a 1 of 16 selection.

4.14 BUS TRANSACTIONS USED WITH THE DH11

4.14.1 Introduction

This section discusses the types of bus transactions used with the DH11. Specific items include:

a. DATI, DATO, and DATOB transactions with the processor as master to read or write into the DH11 registers.

b. DATI transaction with the DH11 as master to obtain a message character (byte) from memory.

c. Generation of an interrupt transaction by the DH11.

This discussion does not include Unibus theory and operation or details of the bus transactions. This information is covered in the *PDP-11 Peripherals and Interfacing Handbook*.

4.14.2 DATI, DATO, and DATOB Transactions (Processor Master)

With the processor as master, the DH11 registers can be read (DATI) or written into on a word basis (DATO) or a byte basis (DATOB). Examples of these transactions are shown below.

DATI Transaction

As an example of a DATI transaction, assume that the processor desires to read the contents of the Next Received Character (NRC) register.

a. The processor places the address of the NRC register on address lines A(17:00) and asserts control lines C1 = C0 = 0. These signals are received by the M7277 module. Address bits A01, A02, and A03 generate signals DATA SOURCE A, B, and C that are sent to the registers multiplexer on the M7278 module to select the 16 bits of the NRC register for transfer to the Unibus data lines.

   The address has been decoded but no control signals can be generated until the processor asserts MSYN L.

b. After asserting the address and control lines, the processor waits a minimum of 150 ns and, if the bus is free (SSYN L is clear), it asserts MSYN L.

c. When the M7277 module receives MSYN L, the address selection logic generates DATA TO BUS H, READ NRC H, and SSYN L. The NRC register output is connected to the input of the registers multiplexer that was selected by signals DATA SOURCE A, B, and C. The multiplexer output is connected to the Unibus drivers on module M7278. Signal DATA TO BUS H is sent to these drivers and enables the NRC to the Unibus data lines D(15:00). Signal READ NRC H is sent to the silo (module M7279) to set a flip-flop (see step h). Signal SSYN L is the DH11's response to the processor that data is available.

d. The processor receives SSYN L and the data. After a minimum delay of 75 ns, the processor strobes the data and clears MSYN L.

e. After another minimum delay of 75 ns, the processor clears the A and C lines.

f. When the DH11 receives the cleared MSYN L signal, the address selector logic clears SSYN L and control signal DATA TO BUS H which clears the D lines.

g. The processor receives the cleared SSYN L signal which signifies the end of the current bus transaction.

h. After completion of the bus transaction (steps a – g), the M7279 flip-flop that was set in step c causes a silo unload operation. This shifts out the just read NRC word and allows the next word in the silo to fall into the last position which is the NRC register.

DATO Transaction

As an example of a DATO transaction, assume that the processor desires to write into both bytes of the System Control Register (SCR).

a. The processor places the address of the SCR on address lines A(17:00), the data on the D lines, and asserts control lines C1 = 1 and C0 = 0. These signals are received by the M7277 module. The address selection logic decodes the address but no control signals can be generated until the processor asserts MSYN L. The data is picked up by Unibus receivers on module M7278, buffered, and sent to the D inputs of the flip-flops that comprise the SCR (module M7289).

b. After asserting the address and control lines, the processor waits a minimum of 150 ns and, if the bus is free (SSYN L is clear), it asserts MSYN L.

c. When the M7277 module receives MSYN L, the address selection logic generates LOAD SCR LOW BYTE H, LOAD SCR HIGH BYTE H, and SSYN L. Signals LOAD SCR LOW BYTE H and LOAD SCR HIGH BYTE H are sent to the M7289 module and clock the data into the SCR. The SSYN L signal is the DH11's response to the processor that it has received the data.

d. The processor receives SSYN L and clears MSYN L. After a minimum delay of 75 ns, the processor clears the A, C, and D lines.

e. When the DH11 receives the cleared MSYN L signal, the address selection logic clears SSYN L and control signals LOAD SCR LOW BYTE H and LOAD SCR HIGH BYTE H.

f. The processor receives the cleared SSYN L signal which signifies the end of the current bus transaction.

DATOB Transaction

As an example of a DATOB transaction, assume that the processor desires to write into the low byte of the System Control Register (SCR).

The sequence of events is the same as that described in the DATO transaction with the following exceptions:

In step a, the processor asserts C1 = C0 = 1 and A00 = 0.

In step c, the DH11 address selection logic (M7277 module) generates LOAD SCR LOW BYTE H only which clocks the SCR low byte (bits 00 – 07).

4.14.3 DATI Transaction With DH11 Master

When the transmitter scanner finds a line that wants to transmit a character, it initiates a request for a non-processor request (NPR) transaction via the M796 Unibus Master Control Module and the M7821 Interrupt Control Module in slot A02. The M7821 requests the NPR, and when it is granted, the DH11 is bus master. The M7821 sends a triggering signal to the M796 which initiates a DATI transaction that transfers the character from memory to the DH11.

The sequence of operation is described below and is referenced to Figure 4-34 which is a block diagram of the M796 and M7821 modules. The DH11 print set contains detailed logic diagrams of the M796 (drawing D-CS-M796-0-1) and M7821 (drawing D-CS-M7821-0-1).

a. The transmitter scanner on M7277 finds a line that wants to transmit a character. The scanner stops which sets the SCANNER STOP flip-flop and asserts SET REQ H.

b. Signal SET REQ H is sent to pin V2 of M796. This is the clock signal for a redefined D type flip-flop that is set to assert REQUEST BUS (1) H.

c. Signal REQUEST BUS (1) H is sent from pin V1 of M796 to pins U1 and V1 of M7821. These pins are the inputs to the A master control section of the M7821 module and when they are high, bus request signal BUS NPR L is asserted at pin U2.

d. If BUS SACK L is clear on the Unibus, the processor asserts the grant signal BUS NPG IN H. This signal is received at pin B1 of M7821.

e. Signal BUS NPG IN H clears BUS NPG OUT H which stops the bus request at this device (DH11). It also asserts BUS SACK L and clears the bus request signal BUS NPR L.

f. The processor receives BUS SACK L and drops the grant signal BUS NPG IN H. When the current bus master completes a data transfer, it clears BUS BBSY L. BUS MSYN L and BUS SSYN L are also cleared. Under these conditions, the M7821 asserts BUS BBSY L at pin D1 indicating that the DH11 is now bus master.

g. Simultaneous with the assertion of BUS BBSY L, the M7821 asserts MASTER NPR L at pin N1.

h. Sig . MASTER NPR L is sent to pins N2 and H1 of M796 to initiate the DATI transaction that brings a character (byte) from memory to the DH11.

i. Signal ADDR TO BUS L is asserted and BUS C1 L and BUS C0 L are both driven high. These C lines indicate the control code for a DATI transaction. The DH11 performs only DATI transactions because the inputs to the C control logic (pins C1 and J2) are permanently connected to ground. Signal ADDR

TO BUS L is sent to the Current Address Register (CAR) on module M7277 to enable the bus drivers and place the current address on Unibus address lines A(17:00). The current address specifies the location (byte) in memory that contains the character to be transmitted.

j. Approximately 200 ns after MASTER NPR L is asserted, the M796 asserts BUS MSYN L on pin E1.

k. The memory has already decoded the current address and, when it receives BUS MSYN L, it places the data (character) on Unibus data lines D(15:00) and asserts BUS SSYN L.

l. The DH11 receives the data via Unibus data lines D(15:00). The byte control logic on module M7277 chooses the proper byte and sends the character to the Data Holding Register leads of the selected UART transmitter awaiting DATA STROBE H. When the M796 receives BUS SSYN L, it asserts DATA WAIT L on pin S2.

m. Signal DATA WAIT L is fed back to pin S1 on M796 and is the trigger input of a 150 ns one-shot. The positive-going trailing edge of DATA WAIT L, which occurs 150 ns after this signal is asserted, triggers the one-shot and it asserts DATA STROBE L at pin T2 of M796 and DATA STROBE H at pin M2 which clocks the Unibus data into the Data Holding Register of the selected UART transmitter.

n. Signal DATA STROBE L is fed back to pin L2 on M796. This signal starts the operation that clears BUS MSYN L, ADDR TO BUS L, BUS C1 L, and BUS C0 L. When these signals are cleared, END CYCLE L is generated at pin N2 of M796 and sent to M7277 to restart the transmitter scanner.

o. When the memory receives the cleared BUS MSYN L signal, it clears BUS SSYN L and the D lines. The cleard BUS SSYN L signifies the end of the current bus transaction.

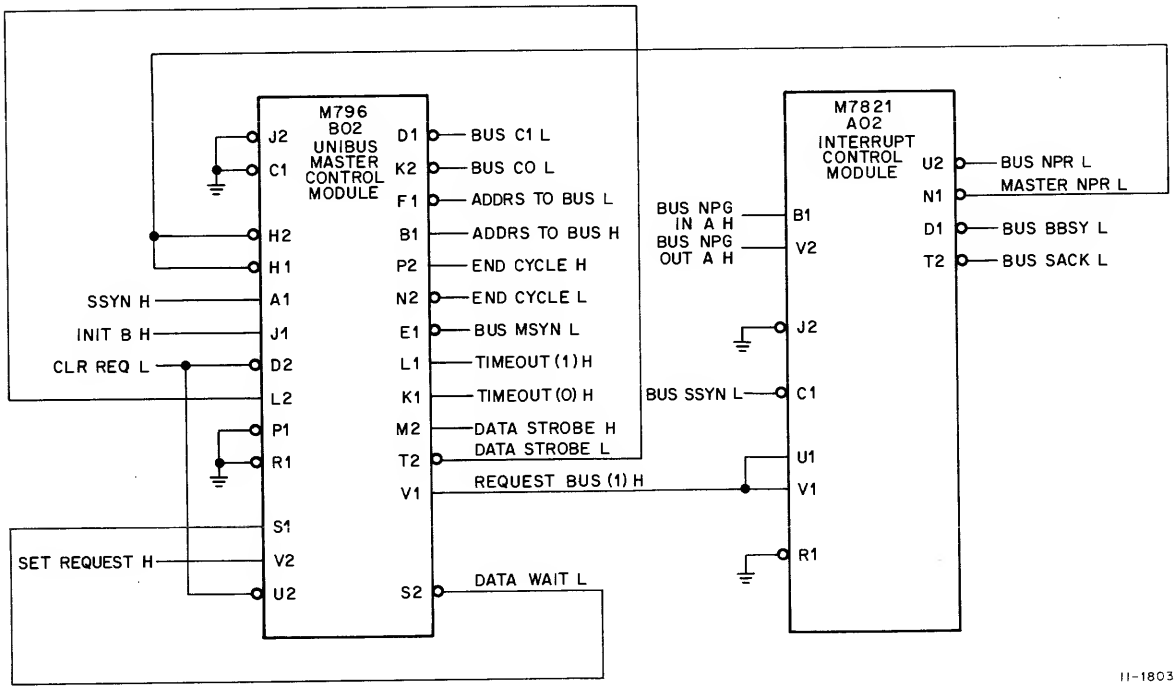


Figure 4-34 Block Diagram of M796 and M7821 Modules Used for DH11 Master Control

If the DH11 addresses non-existent memory, BUS SSYN L is not asserted by the memory. If no BUS SSYN L response occurs within 20 μs of the assertion of BUS MSYN L, signal TIME OUT (1) L is asserted at pin K1 on M796. The DATI transaction is discontinued. Signal TIME OUT (1) L is sent to the System Control Register (SCR) on the M7289. Bit SCR 10 is set and a request for transmitter interrupt is generated, if the transmitter interrupt enable bit (SCR 13) is set. Signal TIME OUT (1) L is also sent to the M7278 module and generates a signal that clears the BAR bit for the selected line. The program clears bit SCR 10 via bit SCR 08. When bit SCR 10 is cleared, it sends a signal to pin D2 of M796 to clear TIME OUT (1) L.

4.14.4 Interrupt Transaction

Four conditions are used by the DH11 to request an interrupt. Two are termed receiver interrupts. One is requested when the program has set the receiver interrupt enable bit (SCR 06) and a character is available in the silo. The other is requested when the program has set the storage interrupt enable bit (SCR 12) and the silo is full at the time the DH11 needs to store an additional character. The remaining two interrupts are termed transmitter interrupts. Both are dependent on the transmitter and non-existent memory interrupt enable bit (SCR 13) being set by the program. One is requested when one or more lines has finished transmission and the other is requested when the DH11 addresses non-existent memory. Both receiver interrupts are requested by RCV INT REQ H and both transmitter interrupts are requested by XMIT INT REQ H. RCV INT REQ H is sent to the A Master Control section of the M7821 Interrupt Module in slot A06. XMIT INT REQ H is sent to the B Master Control section of the same module. Both sections respond to the same bus request level but Section A (receiver interrupt) is electrically closer to the processor so it has the higher priority. A G7360 Priority Selector Card is installed in slot A07 to select the bus request level. Figure 4-35 shows a G7360 card wired for a bus request level of 5.

The M7821 module in slot A06 is used to generate these interrupts. A simplified block diagram of this module is shown in Figure 4-36.

Pin J2 is grounded because this section is used for BR requests. The NPR jumper associated with pin J1 is left in and BUS NPR L is wired to pin J1 to improve NPR latency time.

The interrupt sequence is described below.

a. Assume that a transmitter interrupt has been requested and XMIT INT REQ H is asserted on the M7289 module.

b. XMIT INT REQ H is sent to pins K2 and H2 of the M7281 Interrupt Module. This asserts BUS REQ B L at pin P1 which goes to the G7360 Priority Selector Card and out to the processor as BUS BR5 L. This is a request for bus mastership.

c. The processor examines BUS BR5 L and if it has the highest priority, the processor asserts BUS BG5 IN H provided BUS SACK L is clear. BUS BG5 IN H passes through the G7360 card, the A Master Control section of the M7281 module, through the G7360 card again to pin E1 of the M7281 module where it is identified as BG IN B H. This signal clears BG OUT B H at pin A1 which blocks the bus grant signal and prevents it from reaching any following devices of the same BR level on the Unibus.

d. Signal BG IN B H causes BUS REQ B L to be cleared and BUS SACK L to be asserted at pin T2.

e. The processor receives BUS SACK L and clears BUS BG5 IN H which prevents the issuance of further grants from the processor during this interrupt transaction.

f. When the current bus master completes its transaction, it clears BUS BBSY L and BUS SSYN L. In response to this action, the M7281 asserts its own BUS BBSY L at pin D1 and clears BUS SACK L. When BUS BBSY L is asserted signal B MASTER L is asserted at pin S2 and is sent to pin P2 which is B START INTR L. This asserts BUS INTR L at pin M1 and places the vector address on Unibus data lines BUS DATA 02 – 08 L. The DH11 is now bus master.

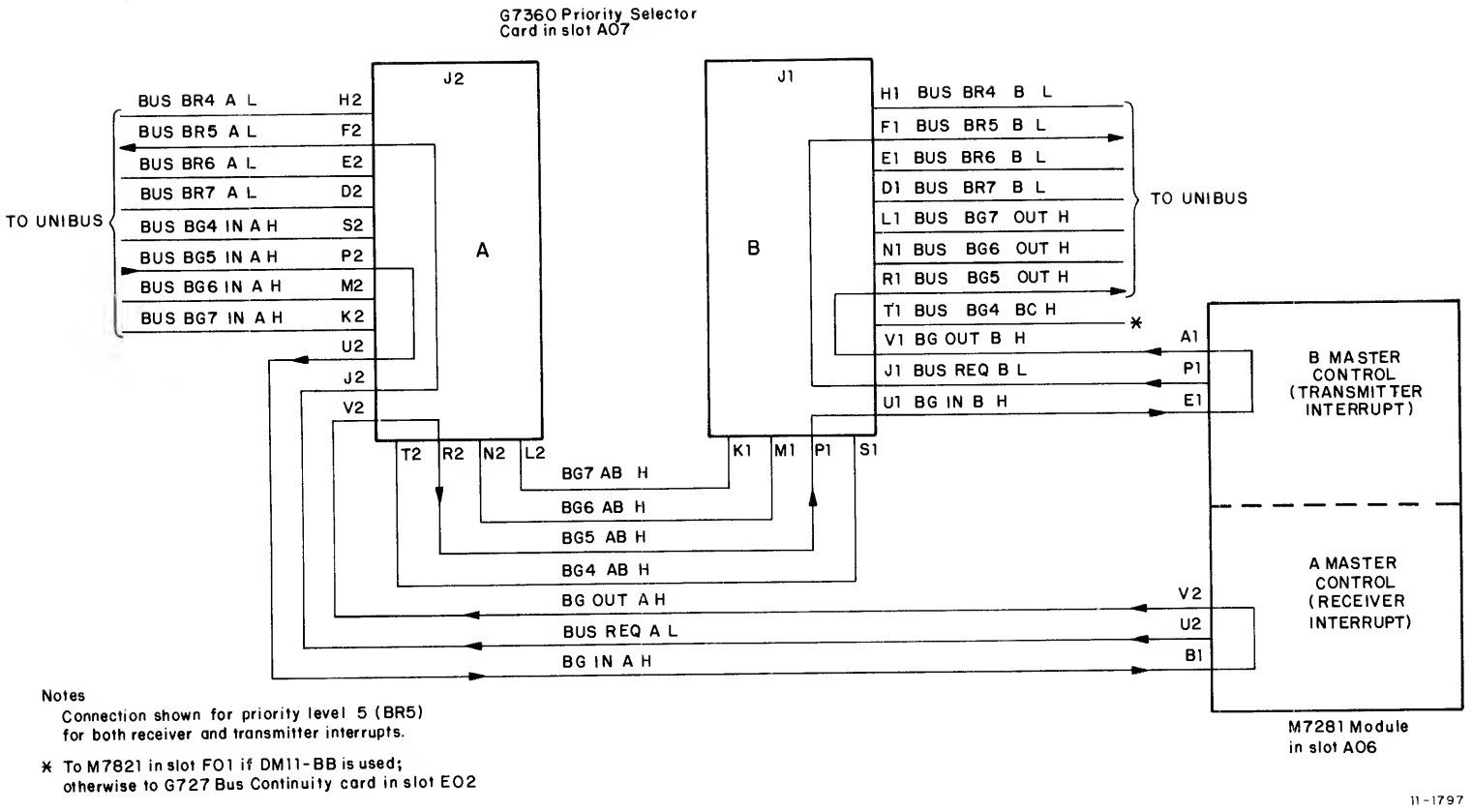


Figure 4-35 DH11 Priority Level Selection Interconnection Diagram (BR5 Selected)

g. The processor receives BUS INTR L, reads the vector address, and responds by asserting BUS SSYN L

h. In response to BUS SSYN L, the M7821 asserts B INTR DONE H at pin M2 which is sent to B MASTER CLEAR H at pin S1. This clears BUS BBSY L, B MASTER L, BUS INTR L, and the vector address. This constitutes active release of the bus to the processor which clears BUS SSYN L when it receives the cleared BUS INTR L signal. The processor goes to the interrupt service routine at the specified vector address.

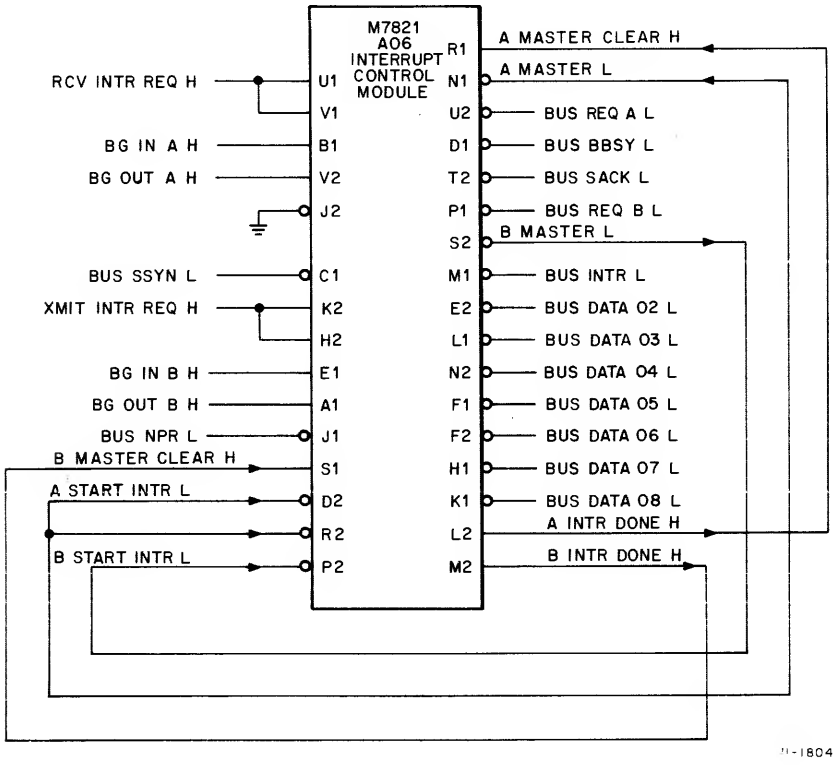


Figure 4-36 Block Diagram of M7821 Module Used for Interrupts

CHAPTER 5
MAINTENANCE

5.1 INTRODUCTION

This chapter provides information for testing and troubleshooting the DH11 using diagnostic programs (MAINDECs) to assist in fault isolation.

The test procedure is divided into two parts: Part 1 verifies the internal logic with the DH11 operating in the maintenance mode; and Part 2 verifies the output interface logic with the DH11 operating on-line (driving signals to a terminal).

Diagnostic programs DZDHA through DZDHK are required. Each program consists of a tape and printout that contains an annotated program listing. The printout contains a descriptive abstract of the purpose of the test and instructions for its use.

Required equipment includes a PDP-11 System and a Tektronix 454 oscilloscope or equivalent.

5.2 INTERNAL LOGIC TESTS (PART 1)

A. Programs Required

DH11 logic tests DZDHA through DZDHI
DH11-AD Modem Control Test DZDHK

B. Procedure

1. For DH11-AA, AB, and AC – Assemble the unit and install the M974 Maintenance Card in location B03 of the distribution panel. The panel does not have to be powered. Other level converter cards should not be installed.

2. For DH11-AD and AE – Assemble the unit and install an H8611 test connector into plugs J1 and J2 on the M5906 module in location AB07 of the DH11 backplane.

3. Using the oscilloscope, verify that a pulse train exists at each of the M4540 Clock Module outputs. The period at each output is listed below. Note that these signals are not square waves.

Pin	Baud Rate	Period
A1	3600	17.4 μs
B1	9600	6.4 μs
C1	7200	8.8 μs
D1	2400	26 μs
E1	2.54 MHz	400 ns
F1	75	800 μs
H1	110	568 μs
J1	1200	52 μs
K1	150	417 μs
L1	300	208 μs
M2	5.068 MHz	200 ns
N1	4800	13 μs
P1	50	1250 μs
R1	200	313 μs
S1	600	104 μs
T2	100	626 μs
U2	1800	34.7 μs
V2	134.5	465 μs

NOTE: Do not attempt to verify the frequency tolerance to a fine degree. Merely verify the presence of the signals and confirm whether or not they are reasonably correct, i.e., not off by a factor of two, etc. These frequencies are crystal controlled (confirm that the crystal is marked 20.277 MHz) and are more accurate than any oscilloscope measurement.

If any of the above signals are not present, check the M4540 divider chain (sheet 2 of the M4540 logic drawing).

4. Load logic test DCDHA. Refer to the diagnostic document for the startup procedure.

5. Run the unit. If errors occur, refer to Paragraph 5.6.2 DZDHA Failures.

6. Repeat steps 4 and 5 above, running DZDHB, DZDHC, DZDHD, DZDHE, DZDHF, DZDHG, DZDHH, and DZDHI. Paragraph 5.5 gives an outline of each of these tests. For each of these tests there is a portion of Paragraph 5.6 that gives a suggested course of action in the case of failure of that test.

7. Run the above diagnostics DZDHA through DZDHI, and correct fault conditions so that all diagnostics run without error for one pass with iterations.

8. If testing a DH11-AD, check out the modem control modules (M7807 and M7808) by running DZDHK. To do this, connect four BC08R cables to J1 and J2 on the M7808 and M7807, and insert the other ends into a H861 test connector. (All four plugs on the H861 are identical.) Run test 0 for 2 passes with iterations.

9. Once the unit has passed test Part 1, proceed to test Part 2.

5.3 ON-LINE TESTS (PART 2)

A. Programs Required

1. DH11 logic test DZDHG

2. DH11 on-line terminal test DZDHJ

B. Procedure (For DH11-AD or AE start with step 4)

1. Connect the H758-A Power Supply to the distribution panel. If an H758-B Power Supply is provided, it must be plugged into 220 V (H739-A and 739-B are equivalent to H758-A and H758-B).

2. Remove the M974 Test Jumper Card from location B03 of the distribution panel.

3. Install the DM11-DA, DB, DC Line Adapter Cards in accordance with the module utilization drawing for the distribution panel. Note that DM11-DA and DB line adapters use the master slots for level converter cards and Bxx slots for cable cards. In the DM11-DC line adapters, the master slots are not used, but rather the level converter card M5xx goes into the A slot above the cable card M9xx associated with that converter.

4. Remove the H8611s from the M5906 module in slot AB07. Connect two BC08S cables from J1 and J2 on the M5906 module to J20 and J17 respectively on the distribution panel.

CAUTION
Read and follow the cable insertion procedure shown in Figure 2-5 of this manual.

5. Refer to Figure 2-6 and step 16 in Chapter 2 for the jumper configurations on distribution panel.

6. Run the DZDHJ on-line test in accordance with the instructions given in that diagnostic. If difficulty is experienced, the transmit portion of the level converters may be checked by running the DZDHG diagnostic and observing the pins of the transmit sections of the level converter cards and the output pins of the cables. Tests are now complete.

5.4 GENERAL CONFIGURATION INFORMATION

5.4.1 Introduction

This section discusses general configuration information primarily related to addressing requirements.

A complete discussion of the DH11 addressing requirements and explanation of the bit assignments and functions for all eight DH11 registers are found in Chapter 3.

5.4.2 DM11-BB Option

If one or more DM11-BB options are ordered along with the DH11s in a system, the DM11-BBs should be installed in the DH11s that have the lowest addresses and vectors.

5.4.3 DM11-DC Line Adapters

If DM11-DC line adapters (four EIA/CCITT lines equipped with dataset control features) are ordered, they should be installed in the distribution panels associated with those DH11s that have been equipped with the DM11-BB Modem Control options.

If less than four DM11-DC line adapters (i.e., 16 lines) are ordered for use on a DH11 equipped with a DM11-BB, use of PDP-11 RSTS programs require that any DM11-DB line adapters ordered for use in this system be installed in that DH11 to bring the total number of level-converted lines to 16. This may mean that one of the DH11s not equipped with DM11-BBs will not be fully equipped with level converters. If so, it should be the DH11 with the highest address that is partially equipped.

5.5 DIAGNOSTIC TESTS SUMMARY

5.5.1 DZDHA DH11 Static Logic Test

Running time: 1 second without iterations, 35 seconds with iterations. Switch settings:

Switch	Action if Set to 1
15	Halt on error
14	Loop in the current test
13	Inhibit error typeout
11	Inhibit iterations
10	Escape to next test on error
09	Loop with current data
02	Restart program at selected test
01	Reselect vector and control register address after program restart

Tests 01 through 10 (octal) test each register of the DH11 for response.

Tests 11 through 14 test to make sure that the SCR, LPR, BCR, and SSR register can be cleared.

Tests 15 through 27 test the ability to set and clear bits 0, 1, 2, 3, 4, 5, 6, 9, 12, 13, and 15 (decimal) of the SCR.

Tests 30 through 34 test the ability in maintenance mode to set and clear bits 7, 8, 10, 11, and 14 (decimal) of the SCR.

Tests 35 through 37 test to make sure that bits 7, 10, 14 can only be cleared while in maintenance mode.

Tests 40 through 56 test the ability to set and clear bits of the Line Parameter Register one at a time.

Tests 57 through 76 test the ability to set and clear the bits of the Break Control Register one at a time.

Tests 77 through 105 test the ability to set and clear bits 0, 1, 2, 3, 4, 5, 15, of the Silo Status Register one at a time.

Tests 106 through 124 set the Line Parameter Register to all 1s and clear the bits one at a time.

Tests 124 through 144 do the same for the Break Control Register.

Tests 144 through 153 do the same for the Silo Status Register bits 0, 1, 2, 3, 4, 5, 15.

If a failure occurs, refer to Paragraph 5.6.1, DZDHA Failures.

5.5.2 DZDHB DH11 Memory Test

Running time: 2 seconds without iterations, 25 seconds with iterations. Switch Settings: Same as DZDHA.

Test 1 is the bus address memory addressing test. It loads each location in the bus address memory with the address of that location. The address is repeated every four bits. The test verifies that each location in the bus address memory was addressed.

Test 2 does the same thing to the byte memories as test 1 did to the current address memories.

Tests 3 through 22 set a 177777 address in bus address memory location 0, verify it, clear it, verify that it is clear, then repeat for location 1, etc.

Tests 23 through 42 do the same for the byte count memory locations.

Test 43 is similar to tests 3 through 22 except that in addition to verifying that the selected location was set to 177777, a check is made to make sure that no data has appeared in any of the other bus address memory locations (they should all be clear except the one set to 177777).

Test 44 is the same as test 43 but uses 125252 as the test word.

Test 45 is the same as test 44 but uses 52525 as the test word.

Tests 46, 47, 50 are the same as tests 43, 44, 45 but are applied to the byte count memories.

Tests 51 and 52 set all locations for the bus address memories (51) or byte count memories (52) to 177777 and then set selected location to 0. No other location should change.

Tests 53, 54, and 55 test the ability to set and clear the memory extension bits.

In case of failure, refer to Paragraph 5.6.2, DZDHB Failures.

5.5.3 DZDHC DH11 Transmitter and Receiver Basic Logic Test

Running time: 23 seconds without iterations, 32 seconds with iterations. Switch settings: Same as DZDHA.

Test 1 sets character available interrupt enable and verifies that no interrupts occur.

Test 2 is the same as test 1, but silo overflow interrupt enable.

Test 3 is the same as test 2, but transmitter done interrupt enable.

Test 4 sets character available interrupt enable, then (in maintenance mode) sets character available, and then verifies that an interrupt occurs.

Test 5 is the same as test 4, but silo overflow.

Test 6 is the same as test 4, but transmitter interrupt enable/non-existent memory.

Test 7 is the same as test 4, but transmitter interrupt enable/transmitter done.

Tests 10 through 27 set byte count for line 0, set BAR bit for line 0, verify BAR bit for line 0 clears, verify transmitter done set. This is done for line 0, then 1, then 2, etc.

Tests 30 through 47 set byte count for all lines to 1, then set BAR bit for line 0, verify that byte count for line 0 goes to 0, that bus address for line 1 is incremented, and that all other byte counts and bus addresses are unchanged. This is done for line 1, line 2, etc.

Test 50 tests the silo maintenance mode by forcing a 1010101010101010 into the silo and verifies that the character available bit is set, that a character available interrupt occurs, that NRC bit 15 is set, and that the 1010101010101010 pattern appears correctly in the Next Received Character (NRC) Register.

Test 51 verifies that the silo up counter counts up correctly.

Test 52 verifies that the silo down counter counts down correctly.

Test 53 tests the silo alarm level for 0, 1, 2, 4, 8, 16, and 32 characters to see that the alarm goes off (i.e., an interrupt occurs) at the proper fill level.

If a failure occurs, refer to Paragraph 5.6.3, DZDHC Failures.

5.5.4 DZDHD DH11 Speed Selection Logic Test

Running time: 15 seconds without iterations, 1 minute 55 seconds with iterations. Switch settings: Same as DZDHA.

Test 1 tests to see that there is a clock for speed 1. It then sends three characters at a selected speed on line 0. It verifies that transmitter done occurs at that selected speed and that the amount of time taken is less at this speed than at the previously selected speed. This is done for 15 (octal), 13 (decimal) speeds at increasing speeds.

Tests 2 through 15 are the same as test 1, but for lines 1, 2, 3, etc., up through line 14 (octal).

Tests 16 through 32 are similar to tests 1 through 15, but for one character, and receiver done is checked and timed rather than transmitter done.

If a failure occurs, refer to Paragraph 5.6.4, DZDHD Failures.

5.5.5 DZDHE DH11 Character Length and Basic Data Test

Running time: 1 second without iterations, 20 seconds with iterations. Switch settings: Same as DZDHA.

Tests 1 through 100 transmit an all 1s character at 9600 Baud, changing first the character length (5 bit, 6 bit, 7 bit, 8 bit) on line 0, then doing the same on line 1, etc.

If a failure occurs, refer to Paragraph 5.6.5, DZDHE Failures.

5.5.6 DZDHF DH11 Single Line Data Test

Running time: 50 minutes 50 seconds without iterations, 52 minutes 25 seconds with iterations. Switch settings: Same as DZDHA.

Tests 1 through 20 transmit all 8-bit characters one at a time on lines 0, 1, 2, etc.

Tests 21 through 40 transmit a block of 400 (octal) characters on line 0; character length is 8 bits. Line speeds start at 50 Baud and are incremented to 9600 Baud. A block of 400 characters is transmitted at each speed. This process is repeated for lines 0 through 17 (octal).

Tests 41 through 60 transmit a block of 400 (octal) characters on line 0; speed is 9600 Baud; character length is 5 bits for the first 400 characters and is then changed to 6 bits, 7 bits, and 8 bits for future blocks of 400 characters. This process is repeated for lines 0 through 17 (octal).

If a failure occurs, refer to Paragraph 5.6.6, DZDHF Failures.

5.5.7 DZDHG DH11 Multi-Line Data Test

Running time: 4 seconds without iterations, 5 minutes 33 seconds with iteration. Switch settings: Same as DZDHA.

Test 1 – In this test the silo alarm level is set to 0. The receiver is to be serviced on a per character basis in interrupt mode. Transmitter interrupts are disabled. A binary count pattern of 400 (octal) characters is sent on all lines. Character length is 8 bits for all lines.

Test 2 – Same as test 1, but all lines are run at 9600 Baud. Silo alarmlevel is set as high as possible. No receiver interrupt servicing, but rather characters are read from the silo as quickly as possible, testing the valid data bit of the Next Received Character Register.

If a failure occurs, refer to Paragraph 5.6.7, DZDHG Failures.

5.5.8 DZDHH DH11 Auto-Echo Test

Running time: 10 seconds without iterations, 2 minutes 40 seconds with iterations. Switch settings: Same as DZDHA.

Tests 1 through 20 enable auto-echo on line 0, transmit an 8-bit character on that line at 9600 Baud, receive and verify that character. This continues until 64 characters have been received. Then disable auto-echo. Exactly one more character should be received. This is done for all 16 lines.

Tests 21 through 40 are similar to tests 1 through 20, but the data checked is a binary count pattern on all lines except that for which the auto-echo is being run. Lines are auto-echoed one line at a time while other transmissions take place.

Test 41 transmits one character on each line with auto-echo enabled. Each line receives 64 characters.

If a failure occurs, refer to Paragraph 5.5.8, DZDHH Failures.

5.5.9 DZDHI DH11 Break and Half-Duplex Test

Running time: 10 seconds without iterations, 3 minutes 25 seconds with iterations. Switch settings: Same as DZDHA.

Tests 1 through 20 test the break facility by first flushing the UART transmitter for a line by transmitting two nulls and setting the break bit for that line. A binary count pattern is transmitted. Only one character should be received and that should be a break character. This is done for each line sequentially.

Tests 21 through 40 set half-duplex on a line. A binary count pattern is transmitted. No characters should be received. This is done for each line sequentially.

If a failure occurs, refer to Paragraph 5.5.9, DZDHI Failures.

5.5.10 DZDHJ Echo Test

This diagnostic contains a test which verifies that all characters (0–377 octal) will echo on each line (0–17 octal) with standard DH11 terminal attachments (TTY 33, 35 or VT05 etc.) using ASCII asynchronous code (110 baud with two stop bits and 300, 600, or 1200 baud with one stop bit).

The starting address is 000200 octal.

Operational switch settings are:

SW15=1	Halt on error
SW13=1	Suppress error typeout
SW02=1	Reselect line number and baud rate
SW00=1	Change parameters at program restart

5.5.11 DZDHK DH11-AD Modem Control Test

This program is a test of the modem control multiplexer used with the DH11-AD option. The program is divided into functional test groups as follows:

Group 0: All line scanner and line multiplexer functions are tested using the H861 test connector.

Group 1: A single line is tested using the modem cable and an H315 test connector.

Group 2: Connect-disconnect tests for 103A modems.

Group 3: Connect-disconnect tests for 202C modems.

The starting address is 000200 octal.

Operational switch settings are:

SW15=1	Halt on error
SW14=1	Loop on current test
SW13=1	Suppress error typeout
SW11=1	Suppress iterations
SW10=1	Escape to next test on error
SW09=1	Freeze data

5.6 DIAGNOSTIC FAILURE ANALYSIS

5.6.1 DZDHA Failures

A. If the following message is received:

```
01346 REGISTER DID NOT RESPOND
ADDRESS
760020
```

this indicates that the PDP-11 processor did not receive a slave sync response from the DH11. The following checks should be made.

1. Was the address entered correctly when responding to the questions asked in the opening dialogue of diagnostic DZDHA? The M7277 module (located in slot 04) is normally supplied with all nine address jumpers in place, making the DH11 address 160000. The following jumper cut table may be of use in verifying that the address cut into the M7277 matches the address typed into the diagnostic.

Jumpers Cut	Address
None	160000
4	160020
5	160040
5-4	160060
6	160100
6-4	160120
6-5	160140
6-5-4	160160
7	160200
7-4	160220
7-5	160240
7-5-4	160260
7-6	160300
7-6-4	160320
7-6-5	160340
7-6-5-4	160360
etc.	

The numbers identifying the jumpers are located on the M7277 etch, right underneath the jumpers. For the set of five jumpers located near the center of the board, the order top to bottom is: 8-11-12-10-9. In the set of four jumpers located near the edge of the board, the order top to bottom is: 7-4-5-6.

2. If the address entered in the opening dialogue of the diagnostic agrees with the jumpered-in address, reload the diagnostic, making sure that there is no check sum error (i.e., that the bus data lights on the computer console are all out when the tape loading finishes). Now try the diagnostic again.

3. If the problem still exists, look at M7277 E72 pin 4. A positive pulse about 1/2 μs long and occurring approximately every 5 μs should be observed when the following toggled-in program is run.

5000/	12706	SET UP STACK	5014/	340	SET UP
5002/	1000		5016/	6	FOR TRAP
5004/	12737	SET UP FOR TRAP	5020/	5737	TEST
5006/	5030		5022/	1600xx	DH REGISTER*
5010/	4		5024/	137	JUMP
5012/	12737		5026/	5020	TO 5020
			5030/	2	RTI

*The number used in location 5022 of the toggle-in program should be the address cited in the error message (Paragraph 5.6.1).

4. If the pulse mentioned above occurs, use it as a trigger source while observing with a second scope channel, E72 pins 1, 2, and 5. There should be a high at each pin during the time that pin 4 is high. If these conditions are met, a negative pulse that is the complement of the positive pulse on pin 4 should appear as the output (pin 6). A shorter negative pulse should appear at E29 pin 10 along with some other pulses. Observing E29 pin 10, without using a trigger source such as E72 pin 4, provides useless information because the slave syncs on the Unibus are observed. The slave sync that corresponds to the positive pulse (but is shorter) on E72 pin 4 is the desired signal.

B. If the following message is received:

```
002312 MASTER CLEAR ERROR
EXP      REC      ADDRESS
000000   771377   760020
```

this indicates that master clear was unable to clear the register named. The following checks should be made.

1. The failure of master clear to clear a register is the result of one of several things. It could be that master clear is not being generated; that the register is not being cleared despite the receipt of an Initialize signal; or that the register is actually being cleared, but that the output of the register is not being properly presented back to the Unibus. The following procedures attempt to ascertain which of these effects is occurring.

   Begin by toggling in the following program which generates a programmed Unibus Initalize:

```
5000/     5    RESET
5002/   137    JUMP
5004/  5000    TO 5000
```

2. Look at M7277 pins EF2 and FV2 for Initialize high, a pulse about 20 ms long that occurs approximately every 60 ms. Also look at pins FR2 and FM2 for an Initialize low pulse. If neither of these pulses can be found, look at pin AA1 to see if Initialize is being generated on the Unibus. If all of these points show the proper signals, generate DH11 Initialize by toggling in the following program:

```
5000/     5    RESET       5006/  160020   THE SCR
5002/ 52737    BIS         5010/     137   JUMP
5004/  4000    BIT 11 IN   5012/    5002   TO 5002
```

3. Check the pins mentioned above for the signals mentioned above (but slightly longer -- about 2.4 μs). If these pulses are not seen at any of the above points, check pin FC1 for negative pulses of 2.4 μs duration. Check EL2 for positive pulses.

4. If M7277 pins EF2, FV2, FR2, and FM2 do show the proper signals, check the following logic:

   SCR not cleared: check M7289 E7, E11, E19, E41, and E50.

   LPR not cleared: check the M7278 E37, E52, E59, and E61.

   BCR not cleared: check the M7278 E38, E51, E60, and E67.

   SSR not cleared: check the M7278 E53, E68, and E69.

5. For the ICs cited above, ensure that the Initialize signal arrives (run the toggle program from step B2 above) and produces the proper clearing action.

6. Run the diagnostic and loop on the current test when reaching the error-producing test. Repeat step 5 above. If the bits cited by the diagnostic as being not cleared are in fact being cleared at the ICs mentioned above, the problem must be in the 74151 multiplexers in the M7278, the 8881s associated with those multiplexers, or in the data source selection leads. On the M7278 print, signal DATA TO BUS HIGH (pin AB1) may be used as a trigger source while looking at the 8881 inputs for the bit that the diagnostic claims is not being cleared.

C. The remainder of the DZDHA test sets and clears the bits of the aforementioned registers one at a time. The following error message is typical:

```
002610    SYSTEM CONTROL REGISTER ERROR
EXP       REC       ADDRESS
000001    000000    760020
```

The following checks should be made.

1. In the case of such a message referring to the System Control Register (SCR), check the M7277 pins CP1 and CT2 for positive pulses while running the diagnostic on a loop of the failing test. These pins should have positive pulses somewhat shorter than 0.5 μs. If these pulses are observed, check M7289 E7, E11, E19, E41, E47, E50 for proper clocking, proper input data, and proper operation. The input data comes from the buffered data buffers on the M7278.

2. In the case of the Line Parameter Register (LPR), check pin EP2 of the M7277 for positive pulses of less than 0.5 μs duration, while looping on the current failing test. Check EH2 for a 300 ns pulse. Also check ED1, EC1, EA1, etc., for the appropriate Control Strobe signal for the line in question. Use the pulse at EH2 as a trigger source. If the appropriate pulses are found, check M7278 E37, E52, E59, and E61 for proper clocking, proper input data, and proper operation. To check input data, use Control Strobe as the trigger.

NOTE

1. **All problems encountered in running DZDHA must be solved before running any other diagnostics.**

2. **Etch shorts, pads that touch, etc., are more common than bad ICs.**

3. **To check input data at a flip-flop, use the clock lead to that flip-flop as a trigger (provided there is a signal on that clock lead), otherwise all of the buffered data signals from the Unibus will be observed.**

3. In the case of the break control register (BCR), check M7277 pin FU1 for positive pulses, and check M7278 E38, E51, E60, and E67 for proper clocking, input data, and operation.

4. In the case of the silo status register, check M7277 pins CP2 and CR1 for positive pulses, and M7278 E53, E68, and E69 for proper clocking, input data, and operation.

5. If proper results are obtained in following the procedure outlined above, check the 74151 multiplexers and 8881s as described in Paragraph 5.6.1 step B6.

5.6.2 DZDHB Failures

A. It is assumed that diagnostic DZDHA has been run successfully.

B. If the following message is received:

```
001376    BUS ADDRESS MEMORY ERROR
EXP       REC       ADDRESS
010421    010420    01
```

this indicates failure to properly read or write the current address memories. If the following message is received:

```
001514    BYTE COUNT MEMORY ERROR
EXP       REC       ADDRESS
010421    010420    01
```

this indicates failure to properly read or write the byte count memories.

C. It is often useful to arrange the PDP-11 console switches to escape to the next test on error by setting switch 10 to the 1 state. After accumulating several error messages and writing down the received and expected data in binary instead of octal, conclusions can be drawn.

Diagnostic Output (Octal)		**Binary Representation**	
Expected	**Received**	**Expected**	**Received**
004376	004356	0000010011111110	0000010011101110
006233	006213	0000110010011011	0000110010001011

Notice that bit 04 is being dropped. If the problem is this simple, or involves a few adjacent bits, go to step I.

D. If the received data is consistently all 0s, it would be wise to look at M7277 pin EN2 DATA TO BUS HIGH while running the following program that reads the current address:

```
5000/   52737   BIS              5016/160026   OF CA TO R0
5002/    4000   BIT 11 IN        5020/   137   JUMP
5004/  160020   THE SCR          5022/  5000   TO 5000
5006/   13737   MOV CONTENTS
5010/  177570   OF SR TO
5012/  160026   THE CA
5014/   13700   MOV CONTENTS
```

If pin EN2 does have a signal (several hundred nanosecond positive pulse every few microseconds), run the diagnostic in a loop on the current (failing) test and look at EN2. The signal should still be there, but not occurring so often. Using this signal as a trigger source, examine the 74151 multiplexers and the 8881 Unibus drivers (M7278).

If the received data is not all 0s but appears to bear little if any relationship to the expected data, follow the procedures outlined in steps E, F, G and H.

E. For current address memory failures, run the toggled-in program from step D. Look at the M7277 E48 pin 1. There should be positive pulses here, each several hundred nanoseconds long and occurring every few microseconds.

F. For byte count memory failures, repeat step E, but use the following toggled-in program:

```
5000/   52737      5010/177570      5020/   137
5002/    4000      5012/160030      5022/  5000
5004/  160020      5014/ 13700
5006/   13737      5016/160030
```

and look for pulses again at M7277 E48 pin 1. This test and the test in step E ensure that the current address and byte count memories are receiving their selection information from the proper point. It is also important to loop the program on the failing test and ensure that bits SCR 00, 01, 02, 03 progress properly from the System Control Register (M7289) to the inputs and outputs of M7277 E48.

G. For current address errors, run the toggle-in program from step D which loads one Current Address Register.

Look at E57 pin 1 for positive pulses of several hundred nanosecond duration. If the pulses are there, use them as a trigger to look at E50 pin 1 for 60 ns pulse that beings 90 ns after the E57 pin 1 pulse begins. This 60 ns pulse is the write enable pulse to the current address memories.

H. For byte count errors, run the toggle-in program from step F which loads the Byte Count Registers.

Look at M7278 pin CJ1 for positive pulses and at M7278 pin BT2 for 60 ns pulses occurring 90 ns after the CJ1 pulses begin. These are the write enable pulses for the byte count memories.

When performing either test G or H, it is important to look at M7277 pin FK1 where 30 ns positive pulses should occur at the conclusion of current address memory write enable pulses and byte count memory write enable pulse. Those 30 ns pulses clear the WRITE CURRENT ADDRESS and WRITE BYTE COUNT flip-flops.

I. If, as explained in step C, a particular bit is incorrect, examine the logic associated with that bit. If the faulty bit is in a current address, examine the M7277. If it is in a byte count, examine the M7278. Run either the toggle program from step D for current addresses or the toggle program from step F for byte counts and check to see that load pulses are reaching the 74193 being used by the bit in question. Also make sure that a write enable pulse is reaching the 7489 involved.

Run the diagnostic, looping on the failing test, while examining the data paths for proper operation. Use the load pulse terminal (pin 11) of the 74193 as a trigger source while looking at data inputs to the 74157 (also be sure that 74157 pin 1 is high) and at the data inputs to the 74193.

5.6.3 DZDHC Failures

A. If the following message occurs:

```
001446    UNEXPECTED INTERRUPT
CONTROL REGISTER CONTENTS
000300    000000
```

a failure in the character available, silo overflow, and transmitter done interrupt circuitry is indicated. This logic is located on the M7289. Loop on the failing test and observe pin DD1, which should be high. E19 pin 6 should also be high. E50 pin 9 and pin 5 should be low.

If DD1 was low, examine the logic of the M7279 Silo Buffer. The M7279 should also be examined if the signal at E50 pin 10 was not a constant high. Signals on E50 pin 4 come from the M7278 E14, and should be constantly high at this point in the testing.

B. If the following message occurs:

```
002202    NO INTERRUPT
```

a failure in the interrupt generation circuitry is indicated. Loop on the failing test. If it is test 4, look at E31 pin 8 on the M7289. If the failing test is test 5, look at M7289 E31 pin 3. If the failing test is test 6, look at M7289 E48 pin 8. If the failing test is test 7, look at M7289 E48 pin 3. In each of the above cases, negative pulses (signal normally high, occasionally going down to 0) should be observed. The signal must not be either always high nor always low, as transitions are necessary for successful operation of the M7821 Interrupt Control module. If negative pulses are found, look at pins DP1 and FM1 for positive pulses. If those pulses are found, try a new M7821 after examining the inputs to the M7821 for proper inputs and proper vector jumpering. Remember that the M7821 jumpers are left in to assert 1s on the bus and removed to assert 0s. For failures in the character available and silo overflow interrupts, be sure that there are positive transitions on M7821 pins U1 and V1. For transmitter done and non-existent memory interrupts, be sure that there are positive transitions on M7821 pins K2 and H2. The M7821 referred to is that located in slot A06.

C. If a failure message such as that below occurs:

```
003150    NO INTERRUPT
003160    TRANSMITTER DONE NOT SET
```

determine the line number and then verify that the BAR bit for that line actually gets set. This may be done by looping on the failing test and examining the BAR register on the M7278. Check for the generation of the transmitter finished pulse by running the following toggle-in program which sets the byte count for each line to all 1s and then to all 0s.

```
5000/   52737   BIS             5020/  160030   TO BC
5002/    4000   BIT 11          5022/     137   JUMP
5004/  160020   IN SCR          5024/    5000   TO 5000
5006/   12737   MOVE
5010/  777777   ALL ONES
5012/  160030   TO BC
5014/   12737   MOVE
5016/  000000   ALL ZEROES
```

Note that a permanent low on M7278 pin AS2 would cause the E14 one-shot to not fire. Pin AS2 should be always high. Look for transmitter finished pulses on pin AR1. Also look at the CLEAR BAR bit signal appropriate to the line in error. Verify that the signal from AR1 causes pin FR2 of the M7289 to go high and/or stay high.

D. If the following failure message occurs:

```
010120    BYTE COUNT ERROR
EXP       REC
777777    000000
```

loop on the current test and examine the BAR bit (M7278) appropriate to the line for which the error is reported. This BAR bit should change back and forth between 1 and 0 during the test looping.

E. In the case of the following message:

```
013330    SILO DATA ERROR
EXP       REC
725252    706400
```

the silo test pattern was not properly received. Loop on the failing test and look at M7278 pin CN2 which should have positive pulses. Observe pin FV2 for 1 μs negative pulses that occur as the result of the CN2 pulses. Look at M7279 pin AR1 for the same pulses that were observed on M7278 pin CN2. Using those pulses as a trigger, look at pins 4 and 9 of the following ICs on the M7279: E2, E7, E12, and E16. These points should be low for at least the duration of the pulses on AR1. Look at pins 7 and 12 of these same ICs for highs occurring for at least as long as the AR1 pulses. These checks confirm that the proper test pattern is being prepared for entry into the silo, that the silo maintenance bit is being set, and that the silo maintenance pulse is being generated.

F. The silo maintenance pulse is used in the DH11 receiver logic to simulate the finding of a Data Available flag, thus causing the silo logic to by cycled.

Observe pin FF1 on the M7289 for the same 1 μs negative pulses that were previously observed on pin FV2 of the M7278. Using these pulses as a trigger source, observe pin AJ2 (LOAD SILO L) where negative pulses should occur about 2 μs after the FF1 pulse. There will be a varying time between the FF1 pulse and the AJ2 pulse because the receiver scanner/receiver logic has to wait for a tick of the 2.54 MHz clock before commencing operation (make sure that there is such a clock signal arriving at the M7289) and this clock is in no way related to the instruction that set the silo maintenance bit and thus generated the silo maintenance pulse that appears on FF1.

Notice that the function of the FF1 pulse is to set SCANNER STOP and thus cause the receiver sequencer (M7289 E21) to generate LOAD SILO L.

G. Confirm the existence of LOAD SILO L pulses at pin BJ2 of the M7279.

H. Be sure that there is a 5.068 MHz (period = 200 ns) clock signal at pin BN1 of the M7279.

I. Be sure that there is -15 V at pin AB2 of the M7279.

J. Check pin BV2 of the M7279 to make sure that the LOAD REQUEST flip-flop is being set and cleared. It is set by the LOAD SILO L pulses (see step G).

K. Check BK2 for 30 ns negative pulses occurring about 170 to 370 ns after LOAD REQUEST sets. (One can use the 5.068 MHz signal as a trigger and turn up the scope intensity). Since these pulses clear LOAD REQUEST, the negative transition of BV2 might also be a good trigger source.

L. Look at pin BK1 for positive pulses about a half microsecond wide. These pulses are the program reading the NRC register and hence cycling a character out of the silo.

M. Observe pin AL1 for negative pulses, occurring throughout the looping on the failing test. If these pulses only occur when starting the program, the silo is probably being filled up, perhaps indicating failure in the unload circuitry.

N. Observe BL1 for positive pulses. These rely upon E9 pin 8 being low at times.

O. Observe BV1 for negative pulses. Trace the effects of these pulses through the M7289 logic.

5.6.4 DZDHD Failures

A. Be sure that the lead entitled Z0 Baud is ground and hence that the TOP BUF Z0 BAUD H and BOT BUFF Z0 BAUD H signals are permanently high. Refer to the M7288 circuit schematic.

B. Check all TOP BUFF and BOT BUFF signals at M7288 E66, E67, E69, E70, E72, E73, E74, E75. Use the table on the first page of the M4540 circuit schematic to determine the proper periods for the various Baud rates. Using an oscilloscope the period can be measured only approximately; however, specific clock signals can be identified to verify that no two are crossed or interchanged.

C. Ensure that the aforementioned signals reach E4 and E2 at the appropriate pins.

D. Looping on the failing tests, make sure that the proper BUFF LPR signals exist at the inputs, that the Control Strobe signal occurs (300 ns), that there is no noise on the Control Strobe signal, and that the outputs of the 74174 and 74175 of the failing line are being properly set.

E. Beware of the fact that the diagnostic detects problems by comparing the time it takes to transmit at one speed with the time it took at a previous speed. When an error is reported, it may be the speed tested prior to the present speed that was in error.

Example: Assume the speeds should be 110, 134.5, 150 and that they are actually 110, 300, 150. The diagnostic will determine that things happened faster at the second speed than at the first speed (300 compared to 110), but when it gets to the third speed (150) it will report an error. The actual problem is the second speed where one finds 300 instead of 134.5.

5.6.5 DZDHE Failures

A. While looping on the failing test, look at CD2 of both UART cards for a 300 ns Control Strobe signal. Check the CH2, CJ1, CF2, CJ2, CF2 pins for proper parameter data.

B. Refer to Paragraph 5.6.7, DZDHG Failures, for further tests.

5.6.6 DZDHF Failures

A. In most cases it should be possible to create failures at a faster rate using the DZDHG diagnostic. If fewer or no failures occur running the DZDHG for a time equal to that during which the DZDHF ran, the problem most likely concerns the loading of line parameters, since the DZDHF changes the line parameters whereas the DZDHG does not.

B. It will generally be beneficial to try the same procedures for troubleshooting DZDHF as DZDHG so it is recommended to follow the procedures below, even if the DZDHF is running.

5.6.7 DZDHG Failures

A. If difficulties occur with one line only, swap M7280 UART cards and see if the problem moves from line 1 (octal) to line 11 (octal), etc.

B. Be sure that the Transmit Strobe signal to the UARTs is long enough. It must be 250 ns or more. Note that this requires an added capacitor on the M796 to generate a wider DATA STROBE. (This capacitor is 100 pF.)

C. If difficulties occur on several lines, but only on one bit, check the buffered data leads, tran data leads, silo inputs, silo outputs, M7278 multiplexers, and M7278 Unibus drivers. Also check the auto-echo switch (M7277 E39 and E42) and the byte switch (M7277 E40 and E43).

D. Receipt of a character that is one lower than that expected may be a failure of the current address up counter system to function properly or a failure of the byte switch (see above).

E. Receipt of a character one higher than expected might be a silo unloading problem; perhaps caused by noise on the read NRC line or perhaps by improper one-shot times.

F. Check all one-shots for accuracy. They should be no more than 20 percent longer or 10 percent shorter than their nominal values. This is particularly true if they are on the short side and the unit is running in high temperatures.

G. Be sure that there is no crosstalk on the control strobe leads.

5.6.8 DZDHH Failures

A. If all of the previous diagnostics have run error-free, failures of this test can only be in a limited area.

B. Loop on the failing test and examine the M7288 Line Parameter Module for the presence of a high on AE ENAB for the failing line.

C. Make sure that the above signal reaches the E22 74154 multiplexer on the M7289. The following toggle-in program sets auto-echo enable on one line and allows the receiver scanner to run continually.

```
5000/   52737   BIS              5022/ 137   JUMP
5002/    4000   BIT 11           5024/5006   TO 5006
5004/  160020   IN SCR
5006/   13737   MOV CONTENTS
5010/  177570   OF SR
5012/  160020   TO SCR
5014/   52737   BIS
5016/   10000   BIT 15 (AE ENAB)
5020/  160024   IN LPR
```

Look at pin 10 of E22 on the M7289 for negative pulses (i.e., the signal is almost always high, but has occasional excursions down to nominal 0 V).

D. Again operate the diagnostic, looping on the failing test. Look at M7289 E18 pins 2 and 6 and E10 pins 3 and 4 for highs. Look at E18 pins 10 and 14 for high. Some of these may be alternately high and low, but what is important now is that they are high at least sometimes.

E. Look at M7289 E14 pin 3 for low pulses, E2 pin 3 for high pulses, E2 pin 6 for low pulses, and E1 pin 4 for high pulses. If E2 pin 3 checks out but the rest do not, check E2 pin 5 for being high at the same time as pin 4 (this should occur). Check E1 pin 5 for being low at the same time as pin 6 (this should occur). If the proper signals cannot be found on E2 pin 5 or E1 pin 5, examine the receiver sequencer E21.

The E21 waveforms can only be observed if the SCANNER STOP flip-flop E44 pin 5 is setting and clearing (i.e., the receiver scanner mechanism is servicing characters). See Figure 4-26.

M7289 E21 Waveforms

Pin	Duration
15	2400 ns
12	2000 ns
10	1600 ns
5	1200 ns
7	800 ns
2	400 ns

F. Trace the AE GO L lead and make sure that it causes M7289 E34 to switch the UART transmitter scan leads and that it causes M7277 E39 and E42 to switch the data source leads for the UART transmitters.

G. If the problem occurs with one line only, try swapping the M7280 UART cards to see if the problem follows – i.e., see if the problem that used to be reported on line 7 (octal) is now found on line 17 (octal).

5.6.9 DZDHI Failures

A. If the following message is received:

001504	MORE THAN 1 CHARACTER RECEIVED	001524	BREAK DATA ERROR
EXP	REC	EXP	REC
000400	000000	720000	700000

it indicates that the break circuitry did not function properly.

B. Check the M7278 E38, E51, E60, and E67 to make sure that the break bit is being set for the failing line. Do this while looping on the failing test. Check M7278 E45, E46, E75, E76 to see if the setting of the break bit produces the appropriate high on the TTL DATA OUT lines. The 7400 gates E45, E46, E75, E76 are normally kept qualified by the high state of the Q outputs from the 74175s that comprise the Break Control Register. Setting of a bit in the Break Control Register brings the appropriate Q output to the low state, disabling the 7400 gate and placing a permanent high on the TTL DATA OUT lines is such that a high = space = 0 = BREAK.

C. If the following message is received: 006244 RECEIVER NOT BLINDED

it indicates that the half-suplex logic did not function correctly.

D. While looping on the failing test, check the M7288 to make sure that the half-duplex bit for the failing line is being set.

E. Check the M7289 to make sure that END OF CHARACTER is being received from the UART that serves the failing line. If in doubt, swap the M7280 UART cards and see if the diagnostic now reports the error on line 11 instead of 1, 12 instead of 2, etc. (The diagnostic reports line numbers in octal).

Also check the M7289 E8, E20, E32, E42 to make sure that the half-duplex enable and end of character signals are disabling the E4, E16, E28, E39 gating appropriate to the line in error. END OF CHARACTER is low while the UART is transmitting a character and comes high very briefly between characters. Loop on a test of a working line if it is desired to see what it should look like.

Make all of the above examinations while looping on the failing test, unless otherwise instructed.

APPENDIX A
FLOATING DEVICE AND VECTOR ADDRESSES FOR COMMUNICATIONS DEVICES

A.1 INTRODUCTION

Starting with the DJ11, new communications devices are to be assigned floating addresses. The addresses for current production devices are to be retained.

The word floating means that addresses are not assigned absolutely for the maximum number of each communications device that can be used in a system.

A.2 DEVICE ADDRESS

Floating device addresses are assigned as follows:

1. The floating address space starts at location 760010 and extends to location 764000 (octal designations).

2. The devices are assigned in order by type: the DJ11 first, followed by the DH11, and then the next device introduced into production. Multiple devices of the same type must be assigned contiguous addresses.

3. The first address of a new type device must start on a modulo 10_8 boundary.

4. A gap of 10_8, starting on a modulo 10_8 boundary, must be left between the last address of one type device and the first address of the next type device. A gap must be left for any device on the list that is not used, if the device following it is used.

5. No new type device can be inserted ahead of a device on the list.

6. If additional devices on the list are to be added to a system, they must be assigned contiguously after the original devices of the same type. Reassignment of other type devices already in the system may be required to make room for the additions.

7. The starting address of the DH11 must be on a modulo 20_8 boundary because the DH11 has eight registers.

The following examples show typical floating device address assignments for communication devices in a system.

Example 1: No DJ11 but two DH11s

760010	Cannot be used for DH11 starting address	
760020	DH11 #0 first address	DH11 requires eight addresses
760022	DH11 #0	
760024	DH11 #0	
760026	DH11 #0	
760030	DH11 #0	
760032	DH11 #0	
760034	DH11 #0	
760036	DH11 #0 last address	
760040	DH11 #1 first address	
760042	DH11 #1	
760044	DH11 #1	
760046	DH11 #1	
760050	DH11 #1	
760052	DH11 #1	
760054	DH11 #1	
760056	DH11 #1 last address	
760060	DH11 Gap (Indicates that there are no more DH11s)	

Example 2: One DJ11, one DH11 and two XX11s (future device with two registers)

760010	DJ11 #0 first address	DJ11 requires four addresses
760012	DJ11 #0	
760014	DJ11 #0	
760016	DJ11 #0 last address	
760020	DJ11 gap	
760030	Cannot be used for DH11 because it is not a modulo 20_8 boundary.	
760040	DH11 #0 first address	
760042	DH11 #0	
760044	DH11 #0	
760046	DH11 #0	
760050	DH11 #0	
760052	DH11 #0	
760054	DH11 #0	
760056	DH11 #0 last address	
760060	DH gap	
760070	XX11 # first address	XX11 requires two addresses
760072	XX11 #0 last address	
760100	XX11 #1 first address	
760102	XX11 #1 last address	
760110	XX11 gap	

A.3 VECTOR ADDRESSES

The floating vector addresses are assigned starting at 300 and proceed upward. The addresses are assigned to devices in the following order: DC11; KL11/DL11-A,B; DP11; DM11-A; DN11; DM11-BB; DR11-A; DR11-C; PA611 Readers; PA611 Punches; DT11; DX11; DL11-C,D,E; DJ11; DH11.

New devices are added as they are introduced into production.

APPENDIX B
PDP-11 MEMORY ORGANIZATION AND ADDRESSING CONVENTIONS

The PDP-11 memory is organized in 16-bit words consisting of two 8-bit bytes. Each byte is addressable and has its own address location: low bytes are even numbered and high bytes are odd numbered. Words are addressed at even numbered locations only and the high (odd) byte of the word is automatically included to provide a 16-bit word. Consecutive words are therefore found in even numbered addresses. A byte operation addresses an odd or even location to select an 8-bit byte.

The Unibus address word contains 18 bits identified as A(17:00). Eighteen bits provide the capability of addressing 256K memory locations, each of which is an 8-bit byte. This also represents 128K 16-bit words. In this discussion, the multiplier K equals 1024 so that 256K represents 262,144 locations and 238K represents 131,072 locations. This maximum memory size can be used only by a PDP-11 processor with a memory management unit that utilizes all 18 address bits. Without this unit, the processor provides 16 address bits which limits the maximum memory size to 64K (65,536) bytes or 32K (32,768) words.

Figure B-1 shows the organization for the maximum memory size of 256K bytes. In the binary system, 18 bits can specify 2^{18} or 262,144 (256K) locations. The octal numbering system is used to designate the address. This provides convenience in converting the address to the binary system that the processor uses as shown below.

17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Address Bit
0	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	Binary
1			1			7			6			0			1			Octal

Address Word Format

The highest 8K address locations (760000–777777) are reserved for internal general registers and peripheral devices. There is no physical memory for these addresses; only the numbers are reserved. As a result, programmable memory locations cannot be assigned in this area; therefore, the user has 248K bytes or 124K words to program.

A PDP-11 processor without the memory management unit provides 16 address bits that specify 2^{16} or 65,536 (64K) locaqtions (Figure B-2). The maximum memory size is 65,536 (64K) bytes or 32, 768 (32K) words. Logic in the processor forces address bits A(17:16) to 1s if bits A(15:13) are all 1s when the processor is master to allow generation of addresses in the reserved area with only 16-bit control.

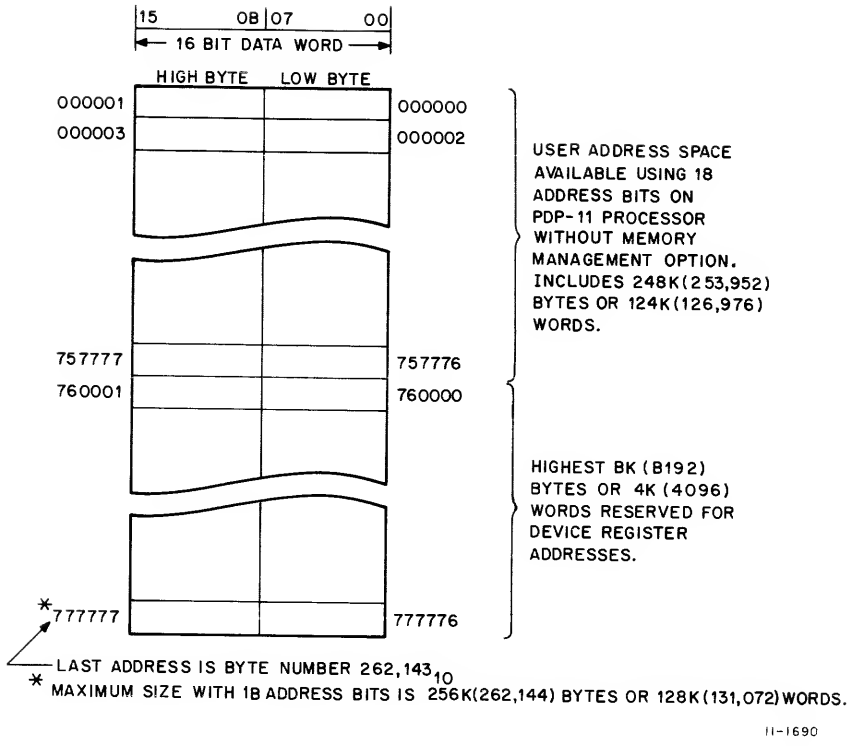


Figure B-1 Memory Organization for Maximum Size Using 18 Address Bits

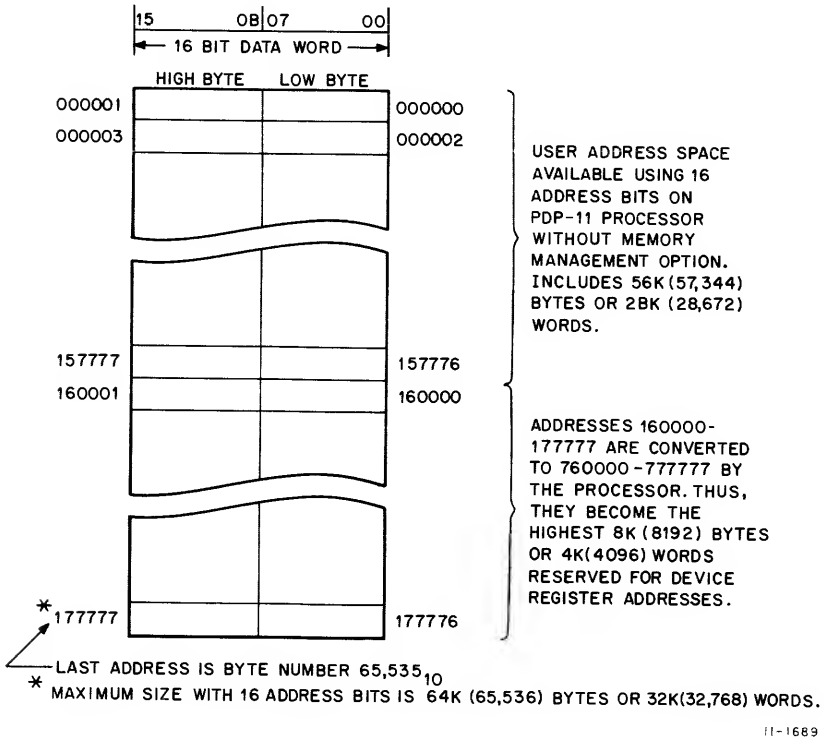


Figure B-2 Memory Organization for Maximum Size Using 16 Address Bits

Bit 13 becomes a 1 first at octal 160000 which is decimal 57,344 (56K). This is the beginning of the last 8K bytes of the 64K byte memory. The processor converts locations 160000–177777 to 760000–777777 which relocates these last 8K bytes (4K words) to the highest locations accessible by the bus. These are the locations that are reserved for internal general register and peripheral device addresses; therefore, the user has 57,344 (56K) bytes or 28,672 (28K) words to program.

Memory capacities of 56K bytes (28K words) or under do not have the problem of interference with the reserved area, because designations less than 160000 do not have a binary 1 in bit A13. No addresses are converted and there is no possiblity of physical memory locations interferring with the reserved space.

PDP-11 core memories are available in 4K or 8K increments. The highest location of various size core memories are shown below.

Memory Size		Highest Location
K-Words	K-Bytes	(Octal)
4	8	017777
8	16	037777
12	24	057777
16	32	077777
20	40	117777
24	48	137777
28	56	157777

APPENDIX C
INTEGRATED CIRCUIT DESCRIPTIONS

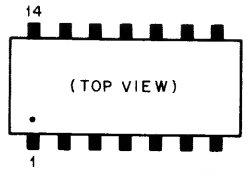
C.1 INTRODUCTION

The MSI and LSI integrated circuits shown in the engineering drawings are discussed in the following paragraphs. The descriptions include a pin/signal designation diagram, simplified logic diagram, and truth table. These descriptions are intended as maintenance aids for troubleshooting to the IC level. Table C-1 lists the ICs by part number, name, and paragraph number.

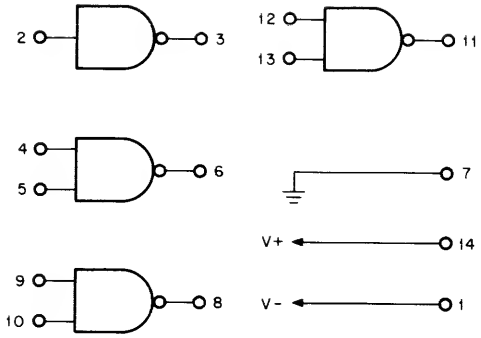
Table C-1
Integrated Circuits

Manufacturer Part Number	Name	Paragraph
1488	Quad EIA Line Driver	C.2
1489	Quad EIA Line Receiver	C.3
3341	4-bit X 64 FIFO Buffer	C.4
4007	Dual-1 of 4 Line Decoder	C.5
4015	Quad D-type Flip-flop	C.6
8266	2-input, 1 of 4 Line Multiplexer	C.7
8271	4-bit Shift Register	C.8
8640	Quad 2 Input NOR, Unibus Receiver	C.9
8838	Quad Bus Transceiver	C.10
8881	Quad 2 Input NAND with Open Collectors	C.11
7442	4 to 10 Line Decoder	C.12
7474/74H74	Dual D-type Flip-flop	C.13
7481	16-bit Active Element Memories	C.14
7485	4-bit Magnitude Comparator	C.15
7489	64-bit Read/Write Memory	C.16
7490	Decade Counter	C.17
7492	Divide by 2 and by 6 Counter	C.18
7493	4-bit Binary Counter	C.19
74121	Monostable Multivibrator	C.20
74123	Monostable Multivibrator	C.21
74151	8 to 1 Line Multiplexer	C.22
74154	4 to 16 Line Decoder	C.23
74155	Dual 2 to 4 Line Decoder	C.24
74157	Quad 2 to 1 Line Multiplexer	C.25
74161	Synchronous 4-bit Counter	C.26
74174/74175	Hex/Quad D-type Flip-flops	C.27
74193	Syncrhonous Up/down 4-bit Counter	C.28
74197	50 MHz Binary Counter/Latches	C.29

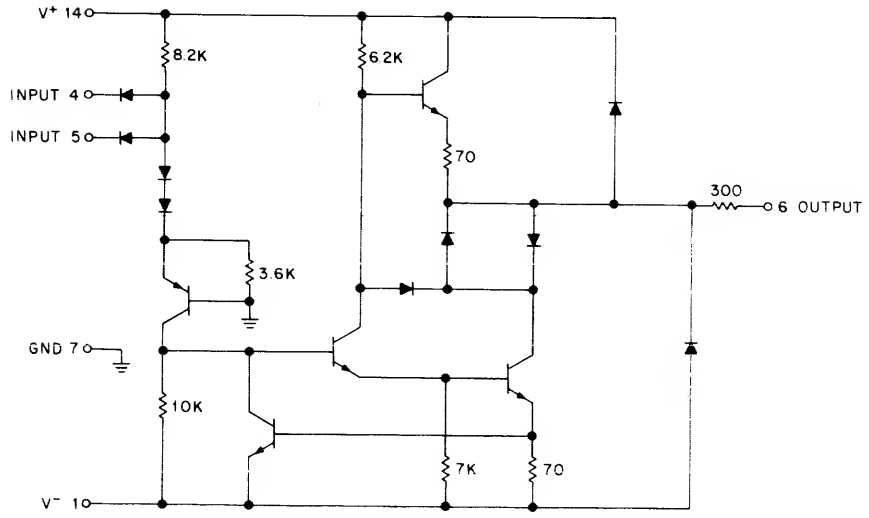
C.2 1488 QUAD LINE DRIVER



11-0486



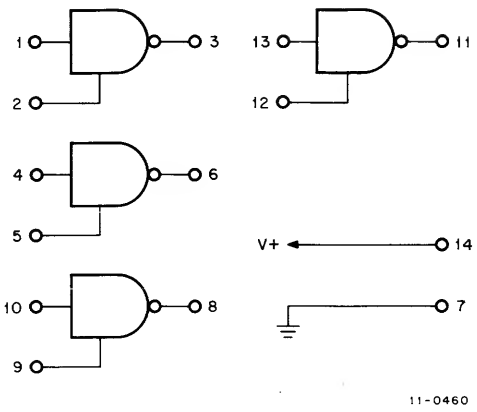
11-0459



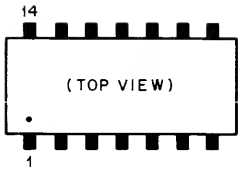
NOTE.
1/4 of circuit shown.

11-0760

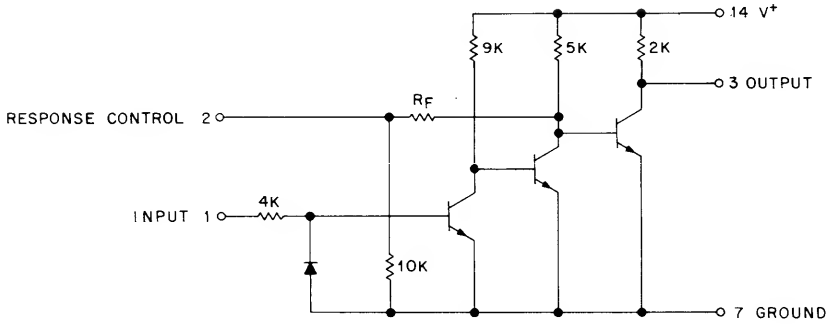
C.3 1489 QUAD LINE RECEIVERS



11-0460



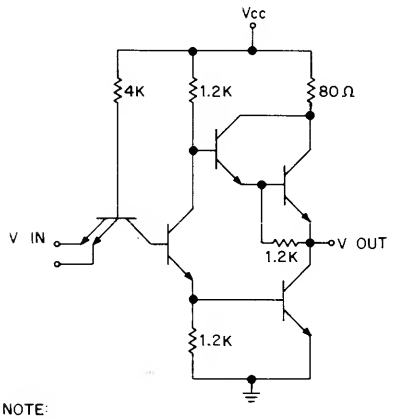
11-0486



NOTE:
1/4 of circuit shown.

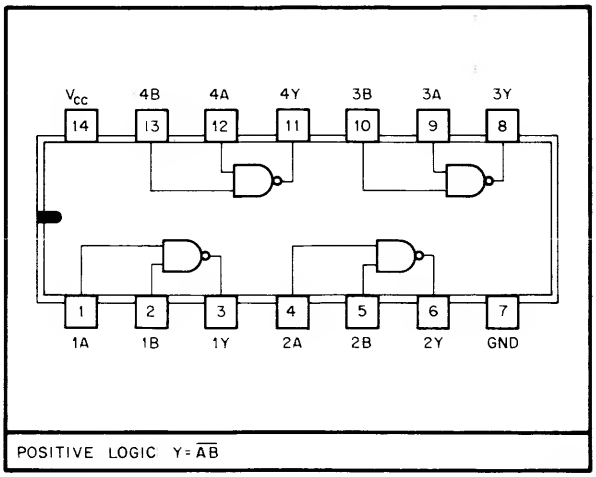
11-0761

7400 QUAD 2-INPUT POSITIVE NAND GATE



NOTE:
Component values are typical.

11-0461



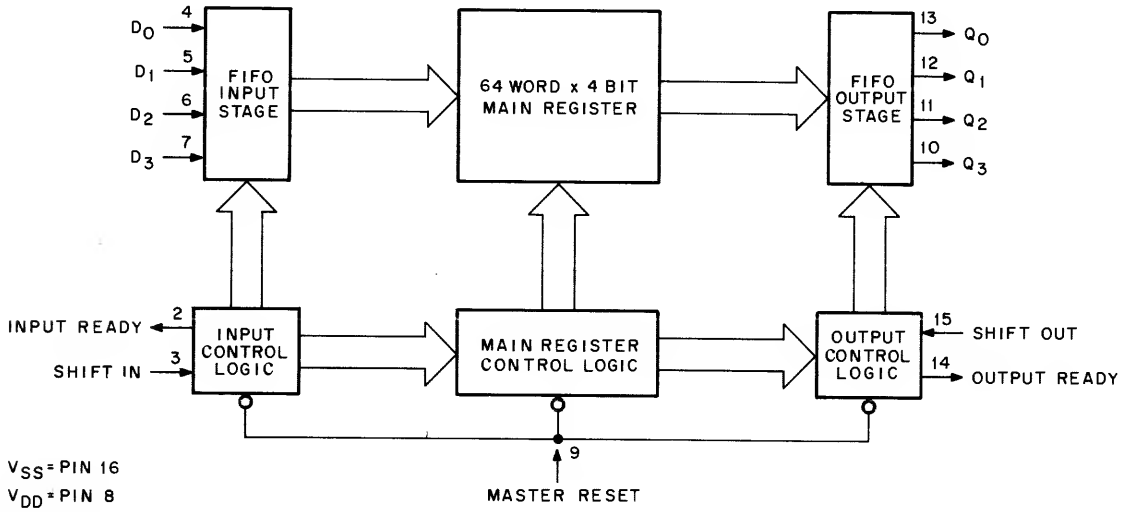
11-0762

C.4 3341 4-BIT X 64-WORD PROPAGABLE REGISTER (FI/FO)

The 3341 is a 64-word X 4-bit memory that operates in a first in/first out (FI/FO) mode. Inputs and outputs are completely independent (no common clocks). The device is used in the DH11 as an asynchronous buffer referred to as the FIFO or silo. When both INPUT READY and SHIFT IN are high, the four bits on D0 through D3 are loaded into the first bit position where they stay until INPUT READY and SHIFT IN go low. This causes the bits to propagate to the second bit position (if empty) where they are propagated to the bottom of the silo by internal control signals.

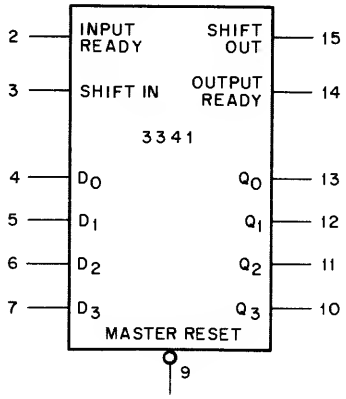
When data has been transferred to the bottom of the memory, OUTPUT READY goes high indicating the presence of valid data. When both OUTPUT READY and SHIFT OUT are high, data is shifted out of the silo. This causes OUTPUT READY to go low. Data is maintained until both OUTPUT READY and SHIFT OUT are low. At this time the bits in the adjacent upstream cell are transferred into the last cell causing OUTPUT READY to go high again. If the silo has been emptied, OUTPUT READY will stay low.

LOGIC BLOCK DIAGRAM



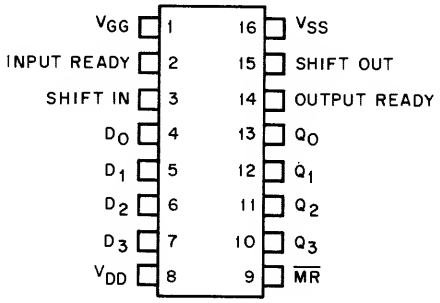
V_{SS} = PIN 16
V_{DD} = PIN 8
V_{GG} = PIN 1

LOGIC SYMBOL



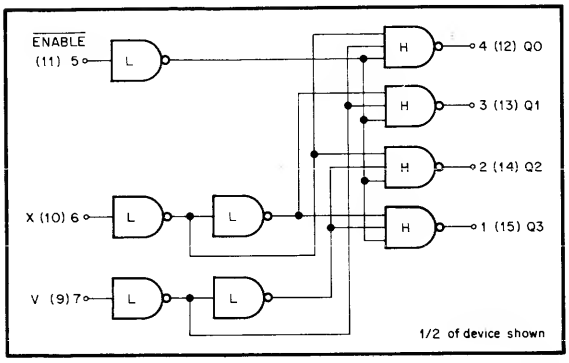
V_{SS} = PIN 16 +5V
V_{DD} = PIN 8 GND
V_{GG} = PIN 1 -12V

PIN CONFIGURATION
(TOP VIEW)



11-1851

C.5 4007 DUAL-BINARY-TO-ONE-OF-FOUR LINE DECODER



11-0742

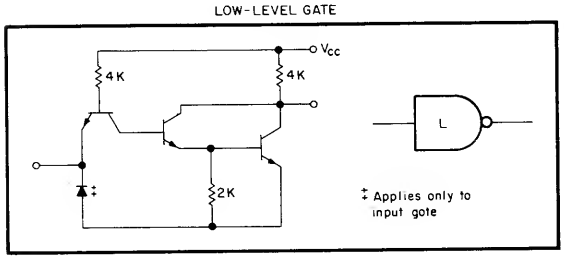
E = 0

TRUTH TABLE

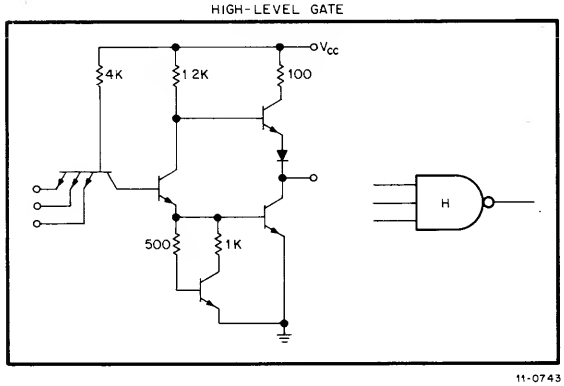
X	Y	Q0	Q1	Q2	Q3
0	0	0	1	1	1
1	0	1	0	1	1
0	1	1	1	0	1
1	1	1	1	1	0

1 = High State
0 = Low State

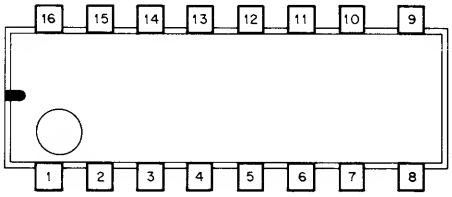
LOW-LEVEL GATE



HIGH-LEVEL GATE

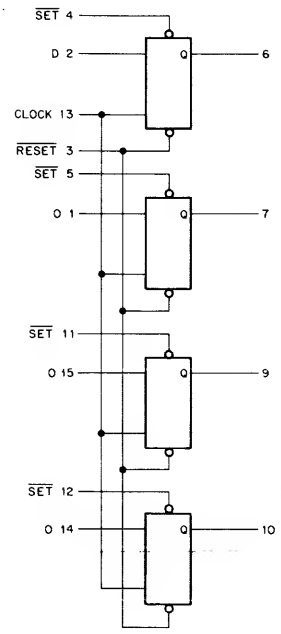


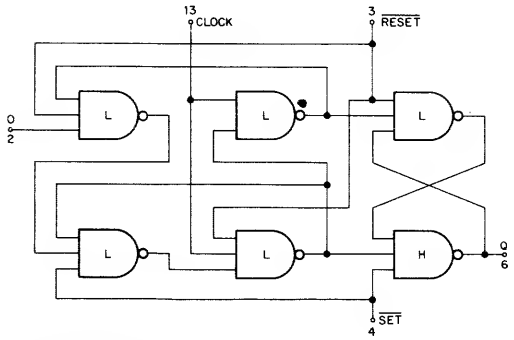
11-0743



11-0744

C.6 4015 QUAD TYPE D FLIP-FLOP

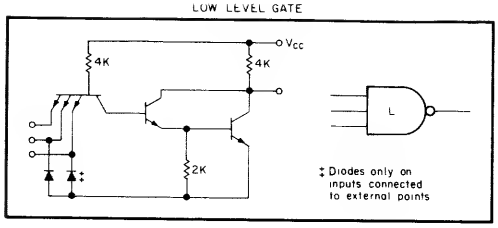




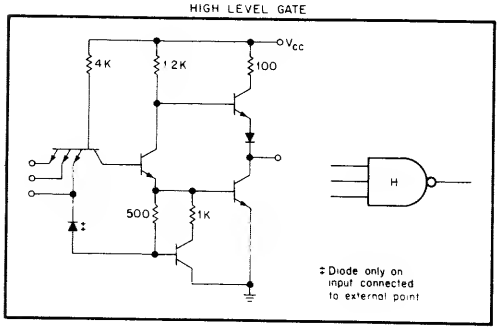
1/4 OF DEVICE SHOWN
CLOCK AND $\overline{\text{RESET}}$ COMMON TO ALL FOUR FLIP-FLOPS
V_{cc} = PIN 16
GND = PIN 8

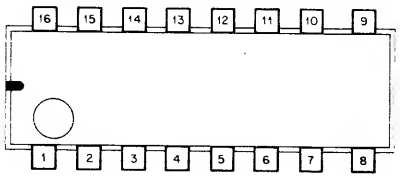
11-0739

LOW LEVEL GATE



HIGH LEVEL GATE





TRUTH TABLE

D	Q_{n-1}	Q_n
0	0	0
0	1	0
1	0	1
1	1	1

Q_{n-1} = time period prior to clock pulse

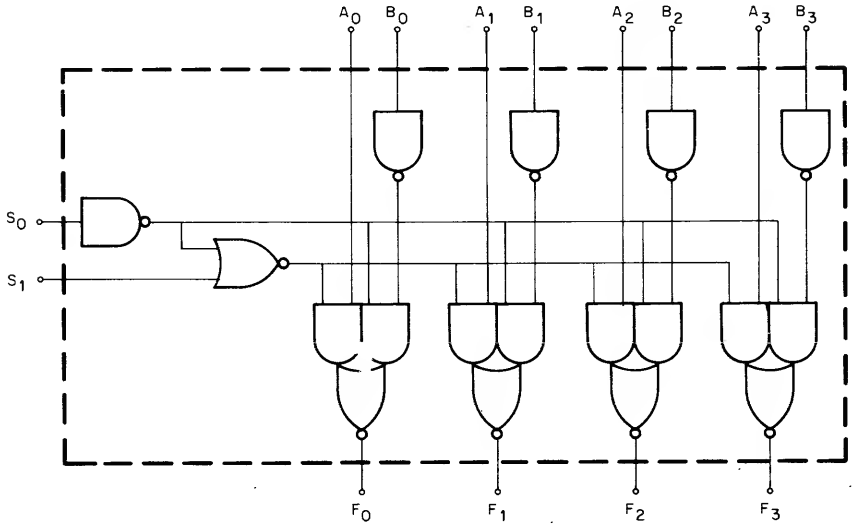
Q_n = time period following clock pulse

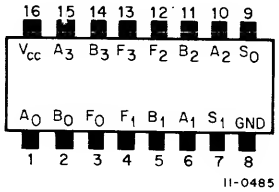
C.7 8266 2-INPUT 4-BIT MULTIPLEXER

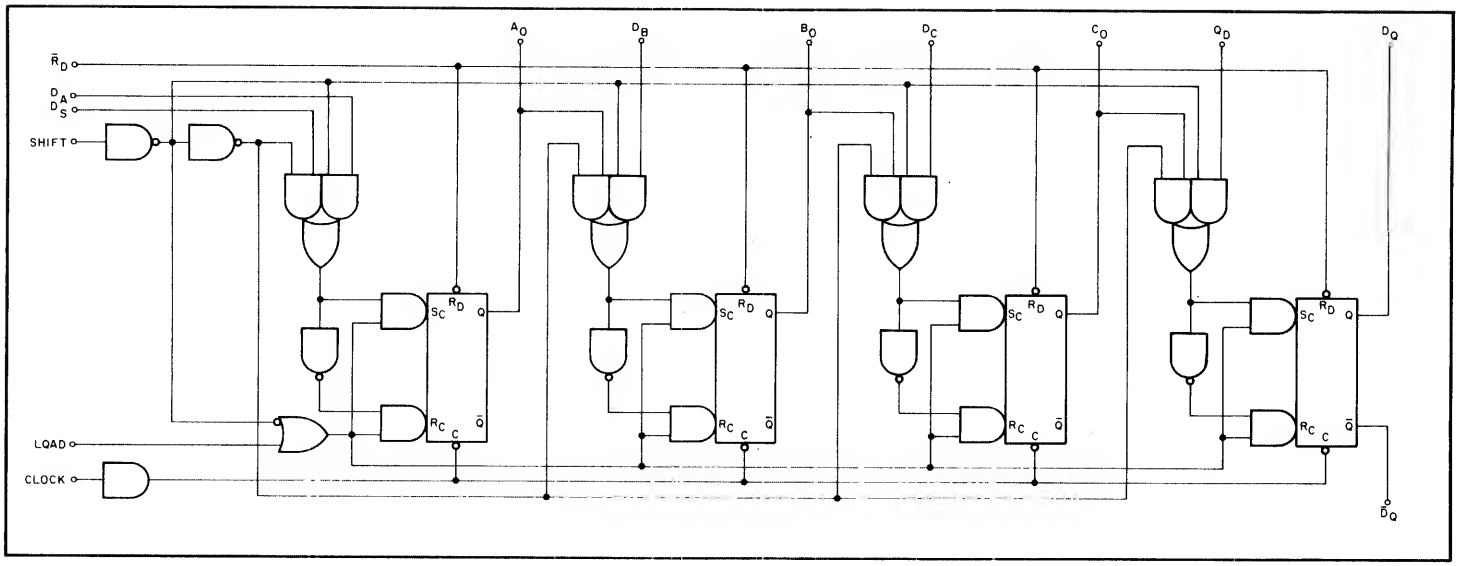
The 8266 is a 2-input 4-bit digital multiplexer that has the capability of choosing between two different 4-bit input sources as controlled by one selection input while the other input is held to 0.

TRUTH TABLE

Select Lines		Output
S_0	S_1	f_n (0,1,2,3)
0	0	B_n
0	1	B_n
1	0	$\overline{A}_n$
1	1	I





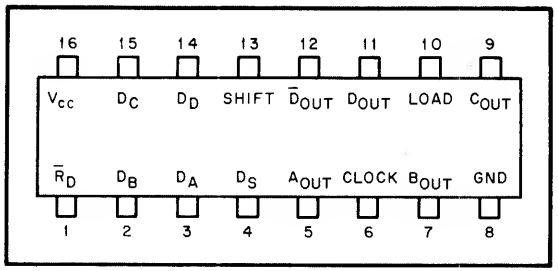


12-0327

TRUTH TABLE

Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1

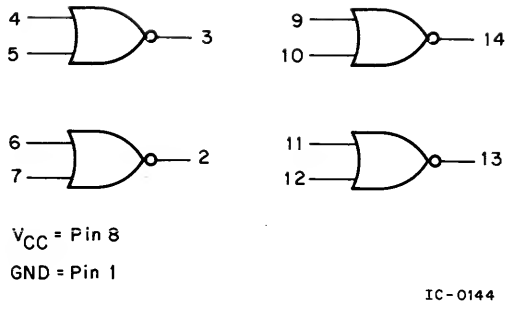
8271B



12-0322

C.9 QUAD 2 INPUT NOR, 8640

Is used as a Unibus receiver.

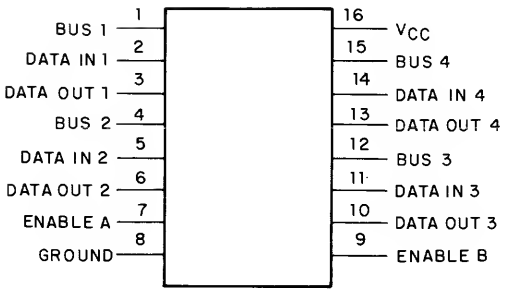


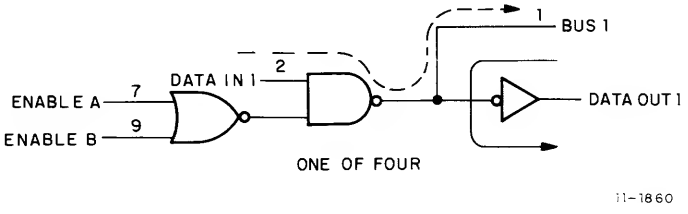
C.10 8838 QUAD BUS TRANSCEIVER

The 8838 consists of four identical receiver/driver combinations in one package for use on the PDP-11 Unibus. Data from the equipment on DATA IN 1, e.g., appearing on pin 2 will be driven out of pin 1 (BUS 1) to the Unibus (if enabled). A BUS 1 signal received from the Unibus on pin 1 will be fed out of pin 3 (DATA OUT 1) to the equipment.

Signal/Pin Designations

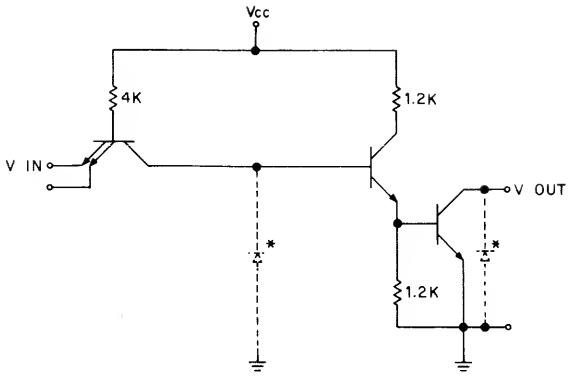
Signal Name	Circuit			
	1	2	3	4
BUS	1	4	12	15
DATA IN	2	5	11	14
DATA OUT	3	6	10	13
ENABLE	A		B	
	7		9	
GROUND	8			





8838 Quad Bus Transceiver

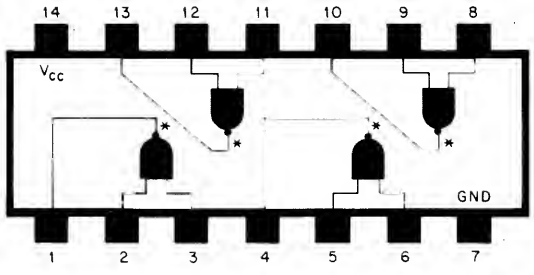
C.11 8881 QUAD 2 INPUT NAND GATES



NOTE:
1/4 of unit shown. Component values are typical.
*ISOLATION DIODE

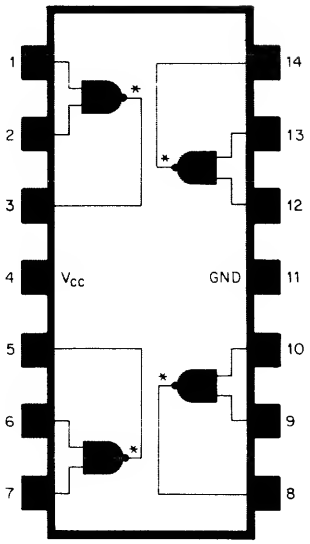
11-0480

A, F PACKAGE



*No pull-up provided

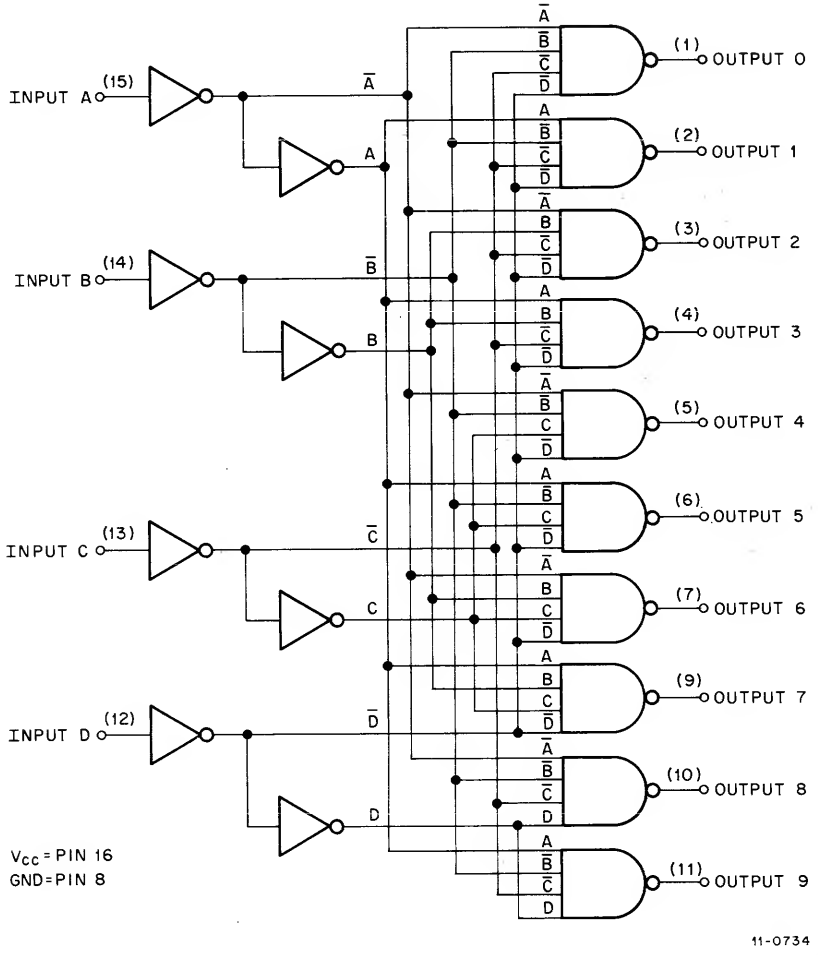
J PACKAGE



11-0758

C.12 7442 4-LINE to 10-LINE DECODER

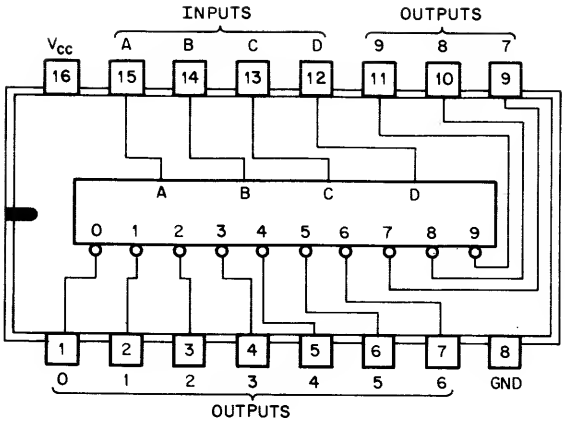
In the DH11, the 7442 is used as a 3-wire binary to octal decoder. Input D is used as a strobe and when it is low, data is taken from outputs 0–7.



TRUTH TABLES

BCD Input				Octal Output							
D	C	B	A	0	1	2	3	4	5	6	7
0	0	0	0	0	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1
0	1	1	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	0
1	X	X	X	1	1	1	1	1	1	1	1

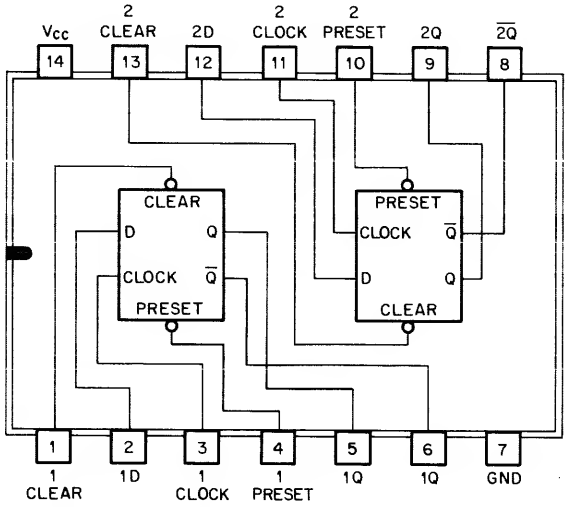
X = Irrelevant



11-0733

C.13 7474/74H74 DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

The 7474/74H74 D-type flip-flops are triggered by the positive edge of the clock pulse. They feature direct-clear and direct-preset inputs and complementary outputs.



POSITIVE LOGIC: LOW INPUT TO PRESET SETS Q TO LOGICAL 1
LOW INPUT TO CLEAR SETS Q TO LOGICAL 0
PRESET AND CLEAR ARE INDEPENDENT OF CLOCK

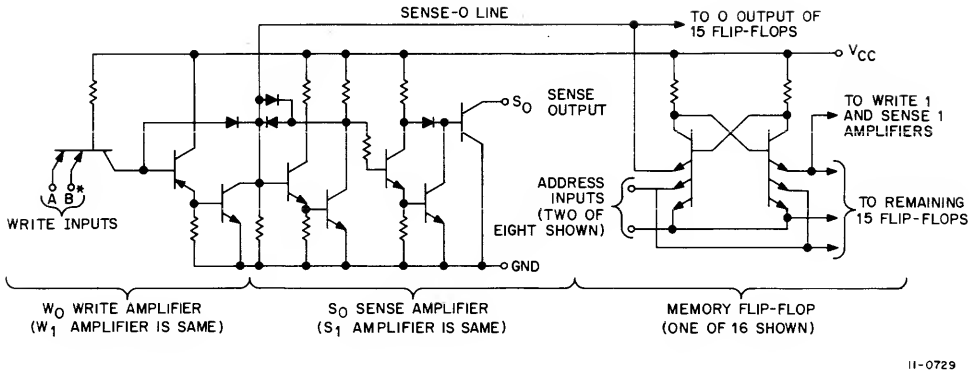
11-0766

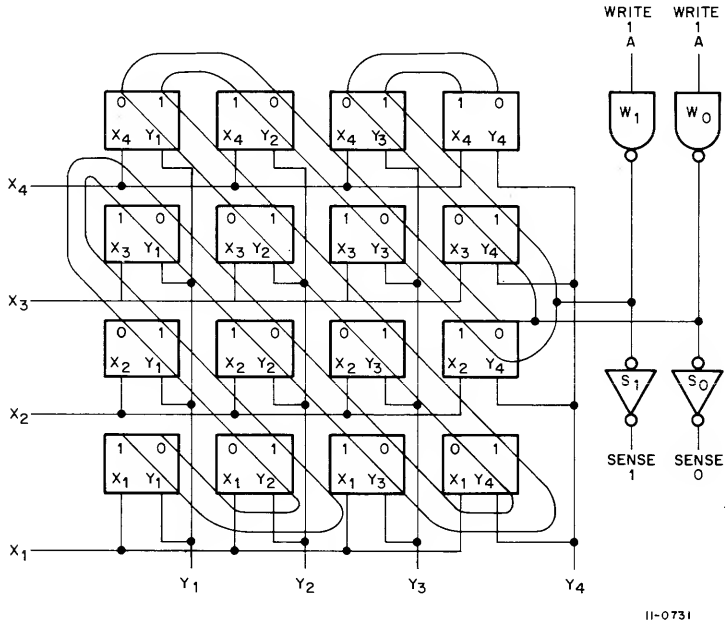
Truth Table (Each Flip-Flop)

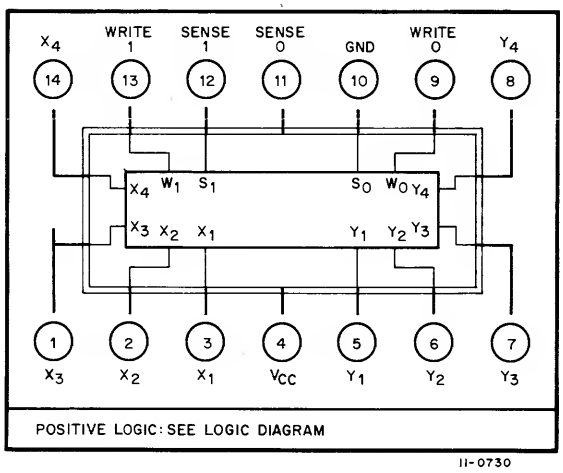
t_n	t_{n+1}	
Input D	Output Q	Output $\overline{Q}$
0	0	1
1	1	0

Notes: 1. t_n = bit time before clock pulse.
2. t_{n+1} = bit time after clock pulse.

C.14 7481 16-BIT ACTIVE-ELEMENT MEMORIES

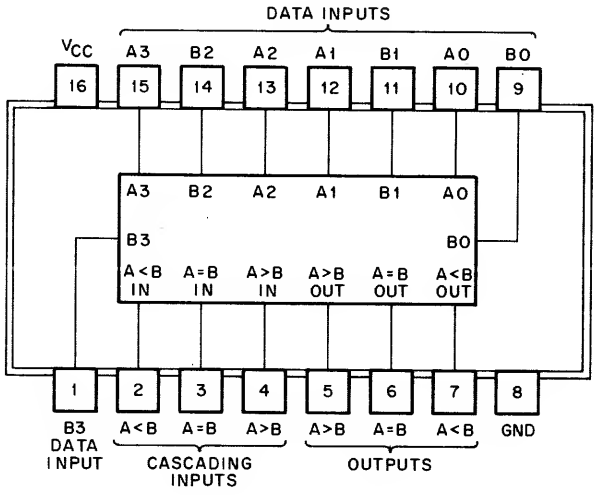






C.15 7485 4-BIT MAGNITUDE COMPARATOR

The 7485 performs magnitude comparison of straight binary or straight BCD codes. Three fully decoded decisions (A > B, A < B, A = B), about two 4-bit words (A,B), are made and are externally available at three outputs.

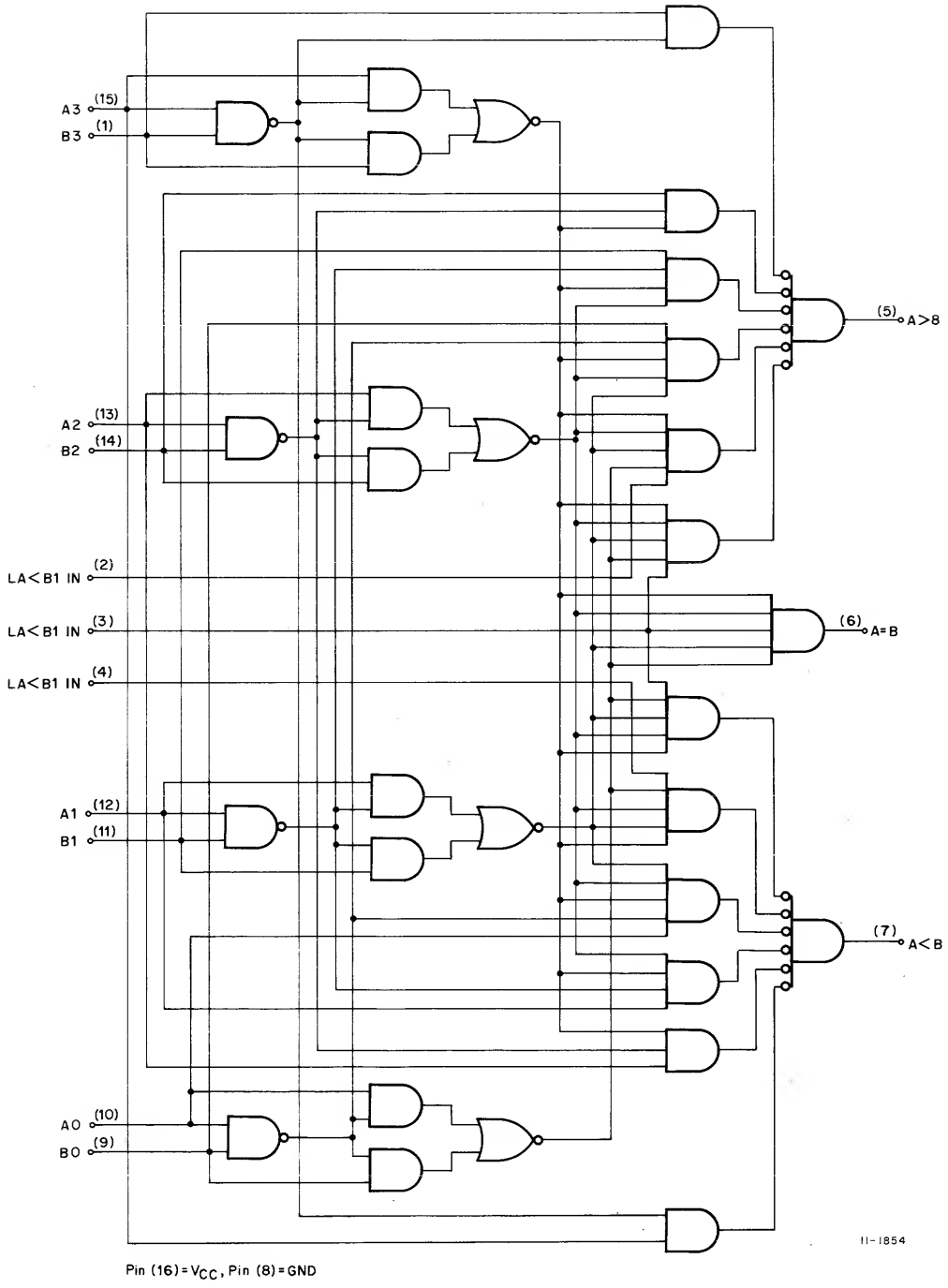


11-2202

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant



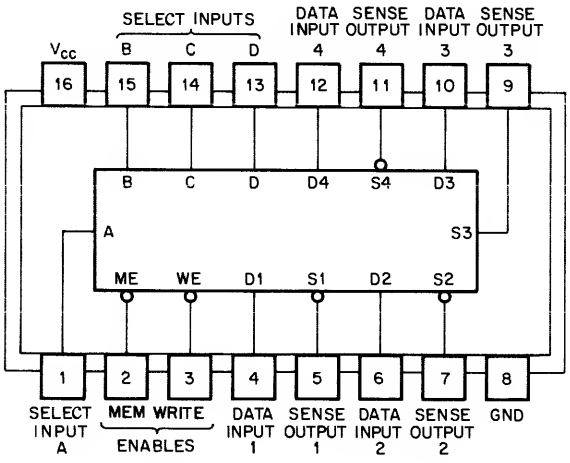
Pin (16) = V_{CC}, Pin (8) = GND

C.16 7489 64-BIT READ/WRITE MEMORY

The 7489 is a TTL array of 64 flip-flop memory cells organized as 16 words of 4 bits each. Each word is addressed in straight binary code with full decoding on the chip. Read out is nondestructive.

Function Table

ME	WE	Operation	Condition of Outputs
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

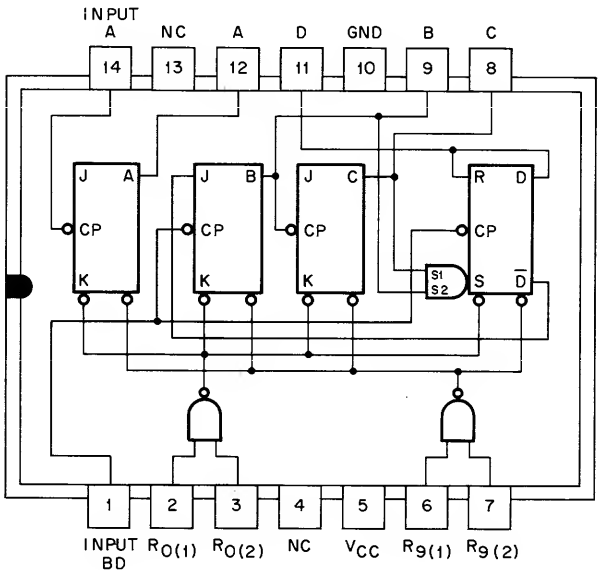


11-1117

C.17 7490 DECADE COUNTER

The 7490 is a decade counter internally interconnected to provide a divide by 2 counter and a divide by 5 counter. In the DH11, the 7490 is used in this way. Input A (pin 14) is the clock for the divide by 2 counter. The output is A (pin 12). Input BD (pin 01) is the clock for the divide by 5 counter. The outputs are B, C, and D. All four reset inputs (pins 02, 03, 06 and 07) are connected to ground to inhibit the preset function.

DUAL-IN-LINE PACKAGE (TOP VIEW)

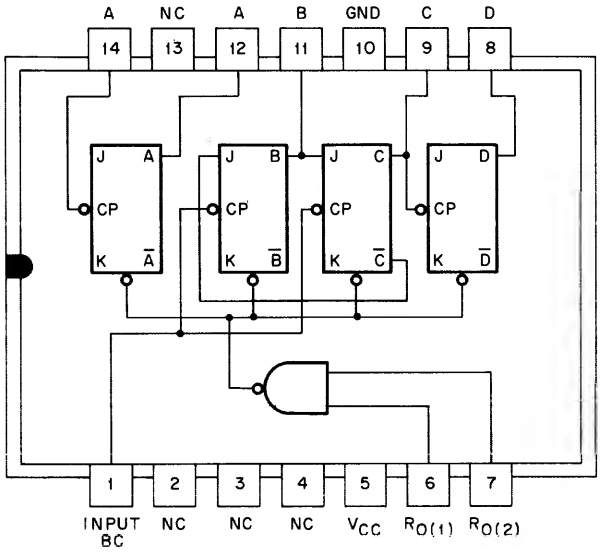


11-1855

C.18 7492 DIVIDE BY 2 AND DIVIDE BY 6 COUNTER

The 7492 is internally interconnected to provide a divide by 2 counter and a divide by 5 counter. Output A (pin 12) provides a divide by 2 count using input A (pin 14) as the clock. Using input BD (pin 01) as the clock, divide by 3 and divide by 6 counts are available at outputs C and D respectively. The Clear inputs (pins 06 and 07) are connected to ground to inhibit the clear function.

DUAL-IN-LINE PACKAGE (TOP VIEW)



11-1856

C.19 7493 4-BIT BINARY COUNTER

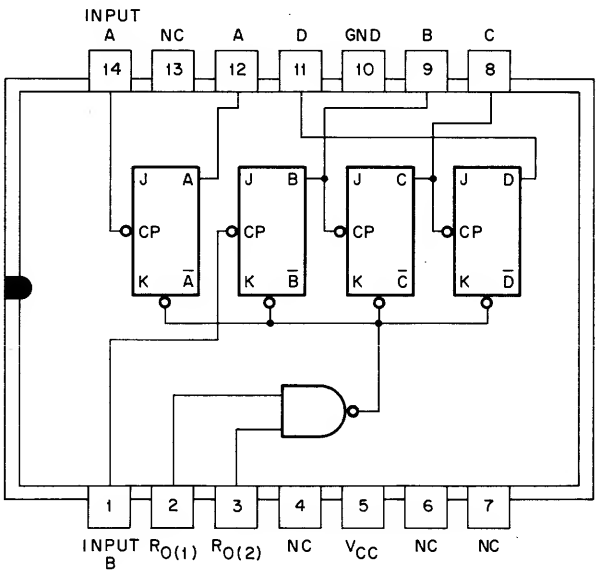
The 7493 is internally interconnected to provide a divide by 2 counter and a divide by 8 counter. Output A (pin 12) provides a divide by 2 count using input A (pin 14) as the clock. Using input B (pin 01) as the clock, divide by 2, 4, and 8 counts are available at outputs B, C, and D, respectively.

The 7493 can be used as a 4-bit ripple-through counter by externally connecting output A to input B and using input A as the clock. Divide by 2, 4, 8, and 16 counts are available at outputs A, B, C, and D, respectively. Both configurations are used in the DH11 and in both cases the clear inputs (pins 02 and 03) are connected to ground to inhibit the clear function. The truth table is shown for the 4-bit ripple-through configuration.

Truth Table (4-Bit Ripple-Through)

Count	Output			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

DUAL-IN-LINE PACKAGE (TOP VIEW)



11-1857

C.20 74121 MONOSTABLE MULTIVIBRATOR

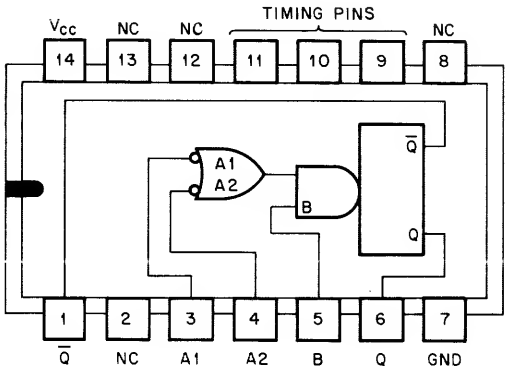
The 74121 is triggered by positive or gated negative-going inputs. The duration of the complementary outputs is determined by external timing components connected to pins 9, 10, and 11.

TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	0	1	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

$1 = V_{in(1)} \geq 2V$

$0 = V_{in(0)} \leq 0.8V$



1. t_n = Time before input transition.
2. t_{n+1} = Time after transition.
3. X indicates that either a logical 0 or 1 may be present.

11-1119

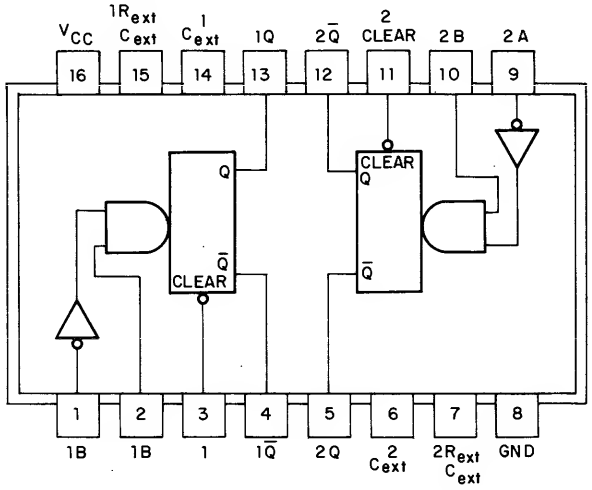
C.21 74123 RETRIGGERABLE MONOSTABLE MULTIVIBRATOR WITH CLEAR

The 74123 Multivibrator provides dc triggering from gated low level active (A) and high level active (B) inputs. It also provides overriding direct clear inputs and complementary outputs. The retriggering capability simplifies generation of extremely long duration output pulses. If the input is triggered before the output pulse is terminated, the output pulse is extended. An overriding clear feature allows any output pulse to be terminated at a predetermined time, independent of timing components.

TRUTH TABLE

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎍
↑	H	⎍	⎍

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic

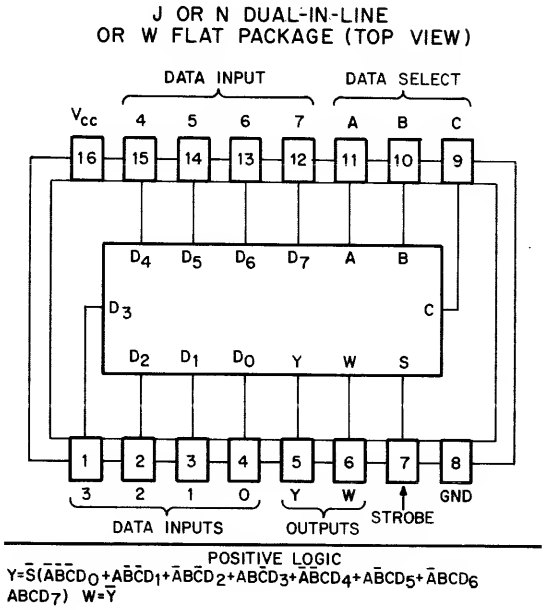
Low input to clear resets Q to low level and inhibits data inputs

11-1864

74123 Retriggerable Monostable Multivibrator With Clear

C.22 74151 8-LINE TO 1-LINE MULTIPLEXER

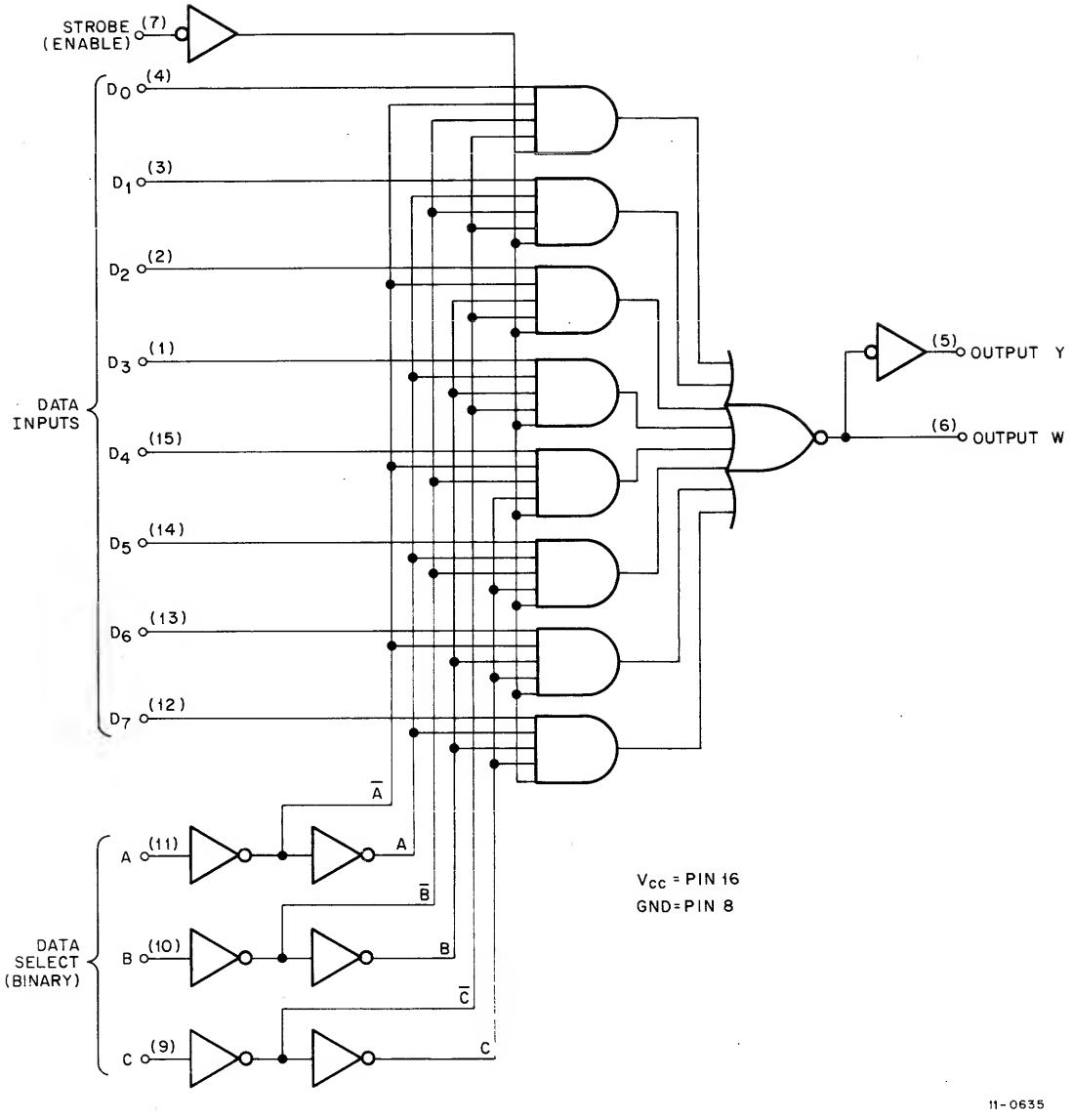
The 74151 selects one of eight data sources for multiplexing the output onto one line. The multiplexer is enabled when the strobe input is low.



TRUTH TABLE

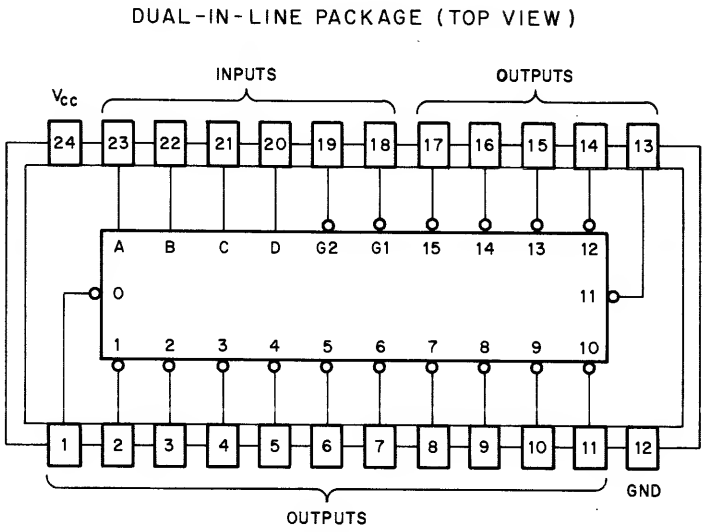
Inputs												Outputs	
C	B	A	Strobe	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
x	x	x	1	x	x	x	x	x	x	x	x	0	1
0	0	0	0	0	x	x	x	x	x	x	x	0	1
0	0	0	0	1	x	x	x	x	x	x	x	1	0
0	0	1	0	x	0	x	x	x	x	x	x	0	1
0	0	1	0	x	1	x	x	x	x	x	x	1	0
0	1	0	0	x	x	0	x	x	x	x	x	0	1
0	1	0	0	x	x	1	x	x	x	x	x	1	0
0	1	1	0	x	x	x	0	x	x	x	x	0	1
0	1	1	0	x	x	x	1	x	x	x	x	1	0
1	0	0	0	x	x	x	x	0	x	x	x	0	1
1	0	0	0	x	x	x	x	1	x	x	x	1	0
1	0	1	0	x	x	x	x	x	0	x	x	0	1
1	0	1	0	x	x	x	x	x	1	x	x	1	0
1	1	0	0	x	x	x	x	x	x	0	x	0	1
1	1	0	0	x	x	x	x	x	x	1	x	1	0
1	1	1	0	x	x	x	x	x	x	x	0	0	1
1	1	1	0	x	x	x	x	x	x	x	1	1	0

When used to indicate an input, x = irrelevant.


STROBE (ENABLE)
(7)
DATA INPUTS
D0 (4)
D1 (3)
D2 (2)
D3 (1)
D4 (15)
D5 (14)
D6 (13)
D7 (12)
DATA SELECT (BINARY)
A (11)
B (10)
C (9)
(5) OUTPUT Y
(6) OUTPUT W
VCC = PIN 16
GND = PIN 8
11-0635

C.23 74154 4-LINE TO 16-LINE DECODER DEMULTIPLEXER

In the DH11 the 74154 is used to decode 4 binary coded inputs into 1 of 16 mutually exclusive outputs when both strobe inputs (G1 and G2) are low.



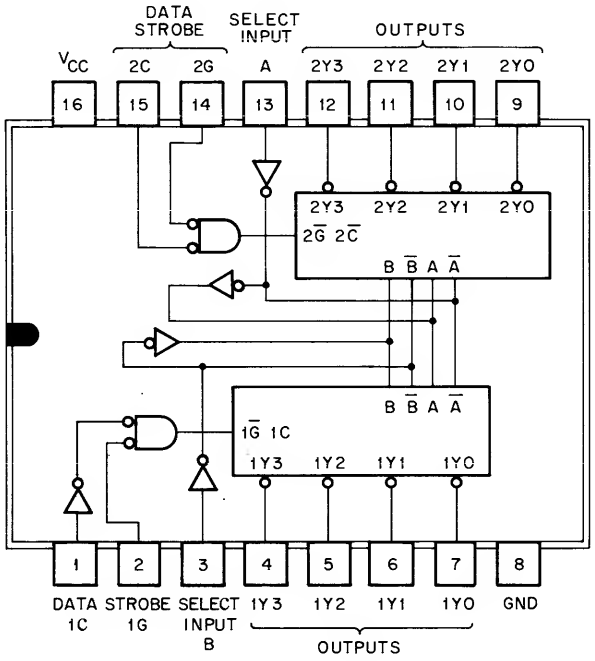
TRUTH TABLE

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high, L = low, X = irrelevant

C.24 74155 DUAL 2-LINE TO 4-LINE DECODER

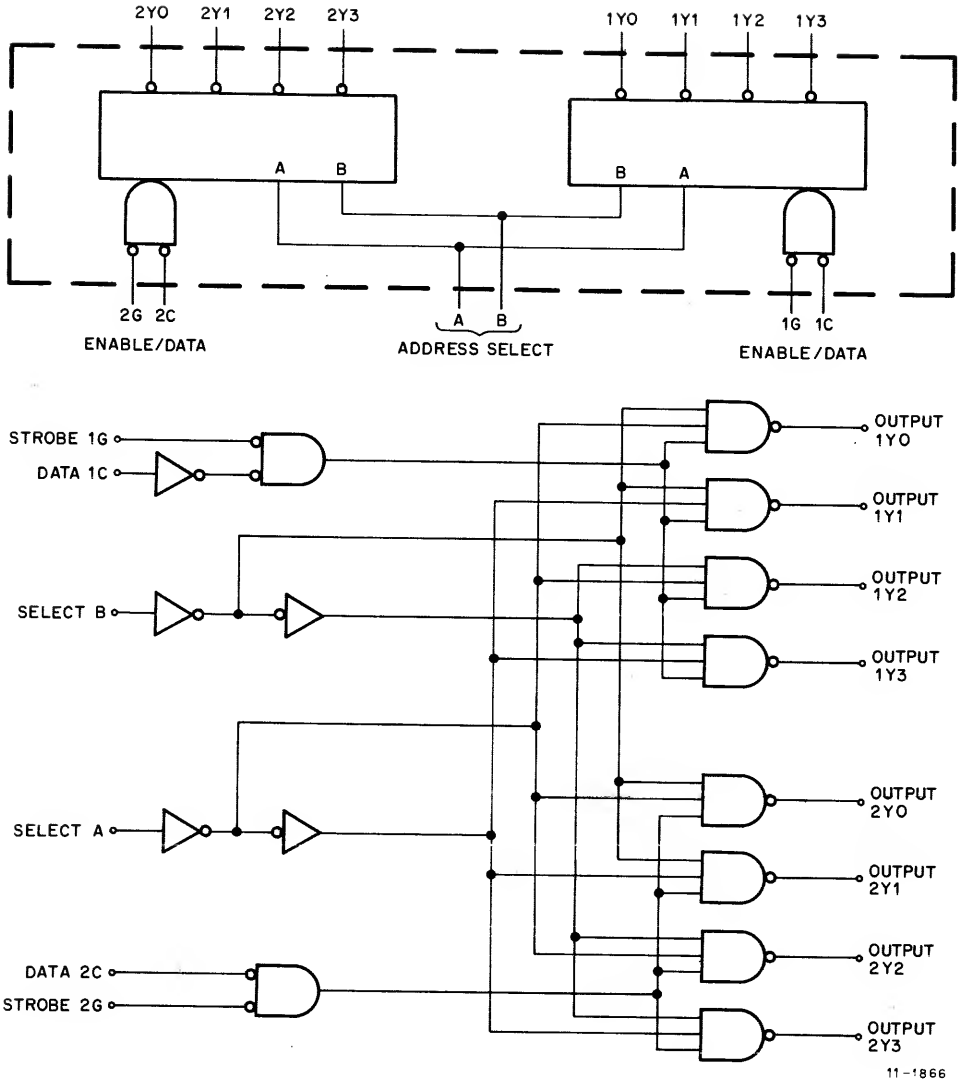
The 74155 consists of two 1-line to 4-line demultiplexers with individual strobes and common binary address inputs. It has several applications, and in the DH11 it is connected as a 3-line to 8-line decoder. The two strobe inputs are connected together and the third select input (Select C) is obtained by connecting the two data inputs together.



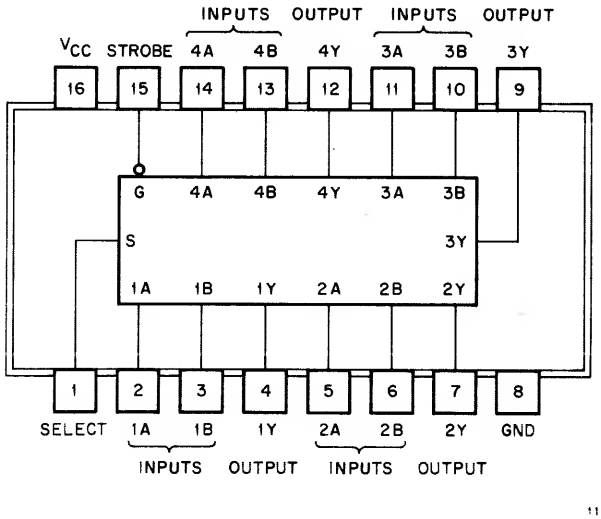
3-Line To 8-Line Decoder

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C*	B	A	G**	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H'	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

* Inputs 1C and 2C connected together
** Inputs 1G and 2G connected together



C.25 74157 QUAD 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

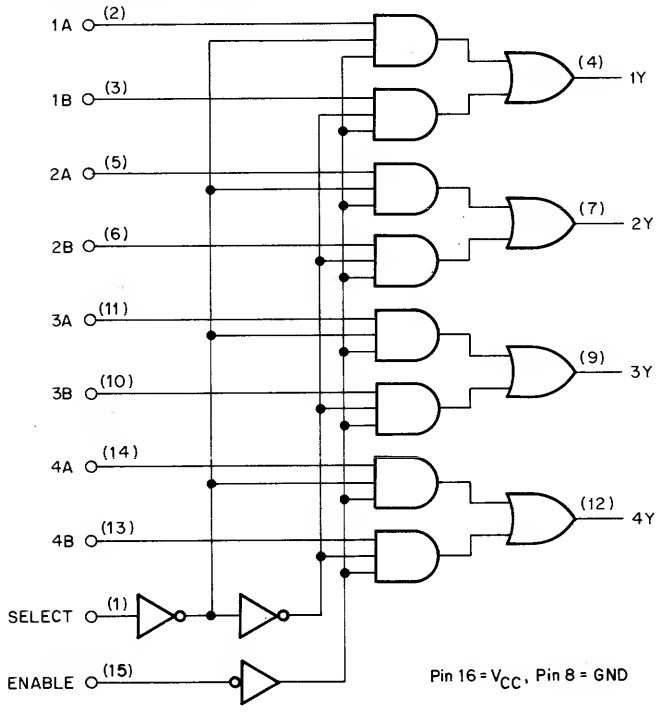


TRUTH TABLE

INPUTS			OUTPUT Y	OUTPUT W
ENABLE	SELECT	A B	74157	74S158
H	X	X X	L	H
L	L	L X	L	H
L	L	H X	H	L
L	H	X L	L	H
L	H	X H	H	L

H=High level, L=Low level, X=Irrelevant

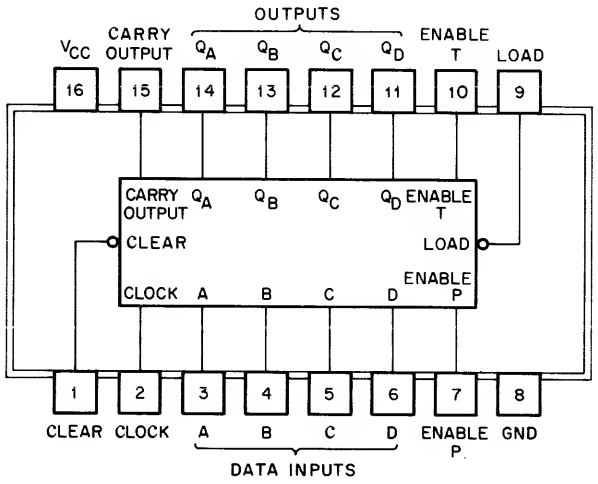
74157 LOGIC DIAGRAM



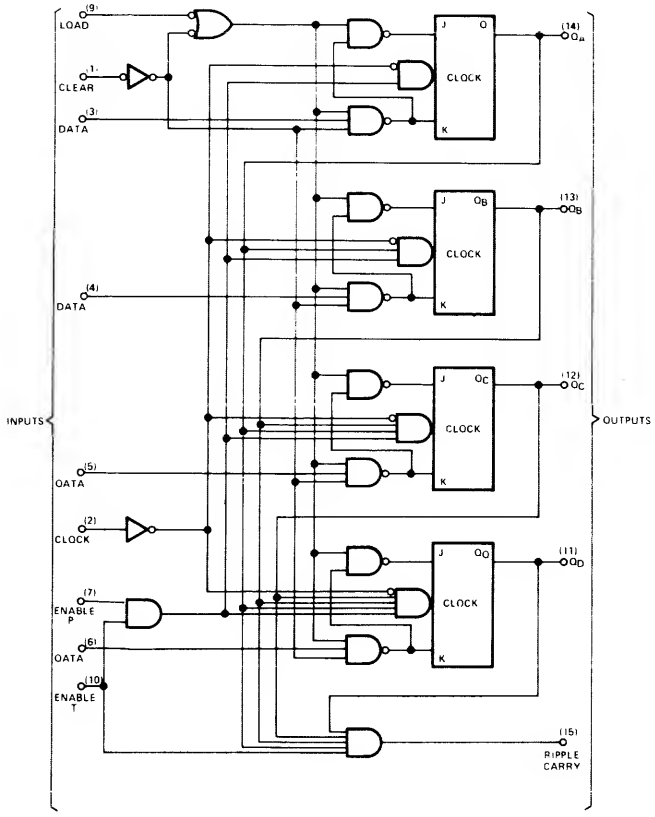
11-1131

C.26 74161 SYNCHRONOUS 4-BIT COUNTER

In the DH11, the 74161 counters are used to provide a divide by 11 function and a divide by 7 function. These functions are obtained by presetting the data inputs. The carry output (pin 15) is fed back to the load input (pin 09) to preset the counter on the count of 15. In both configurations, the clear input and both count enable inputs (Enable T and Enable P) are connected to +3 V. This keeps the counter enabled and disables the clear function.



11-2201



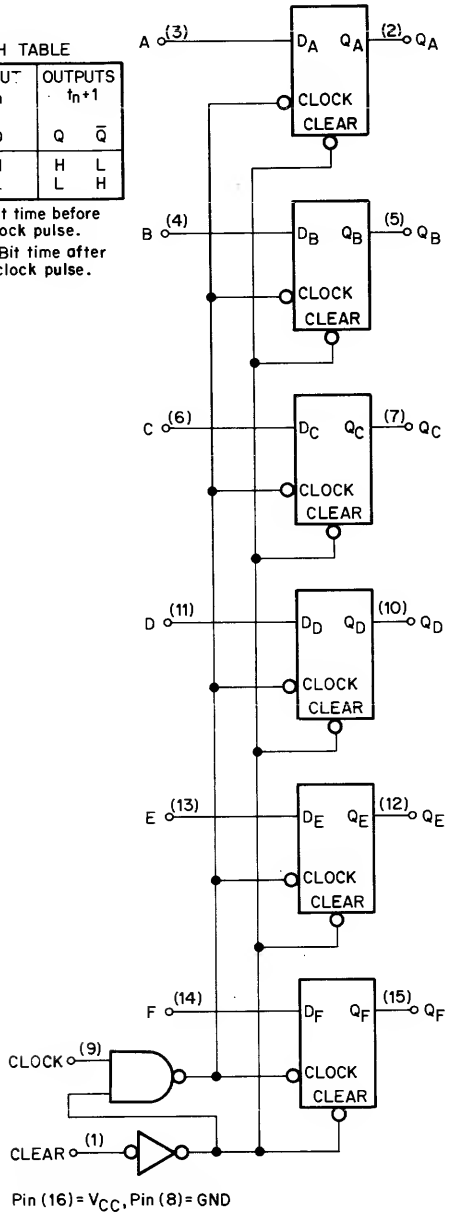
C.27 74174 HEX/74175 QUAD D-TYPE FLIP-FLOPS WITH CLEAR

The 74174 contains six flip-flops with single-rail outputs (Q only). The 74175 contains four flip-flops with double-rail outputs (complementary Q and $\overline{Q}$). Both devices have common clock and clear inputs.

TRUTH TABLE

INPUT t_n	OUTPUTS t_{n+1}	
D	Q	$\overline{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.



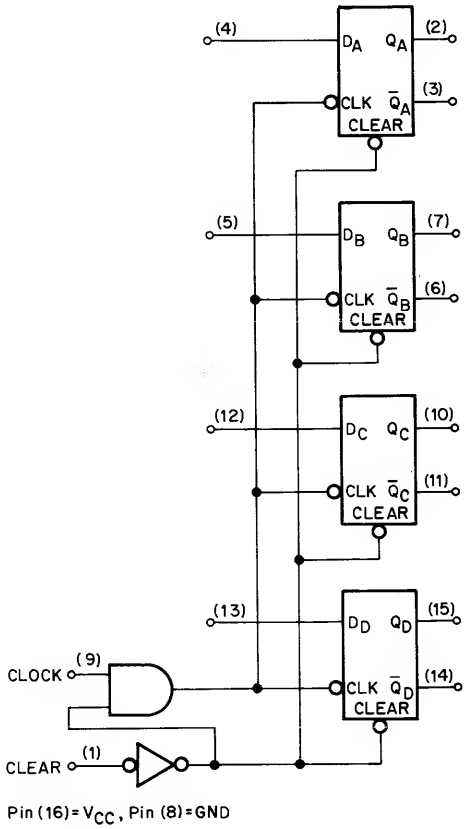
11-1112

74174 Diagram

TRUTH TABLE

INPUT t_n	OUTPUTS t_{n+1}	
D	Q	$\overline{Q}$
H	H	L
L	L	H

t_n = Bit time before clock pulse.
t_{n+1} = Bit time after clock pulse.

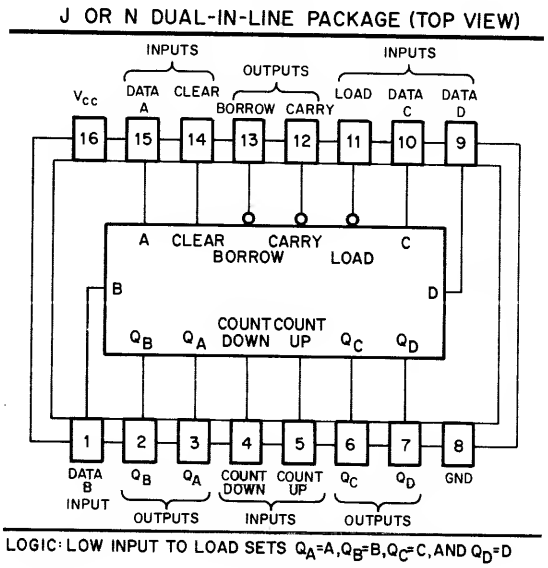


11-1113

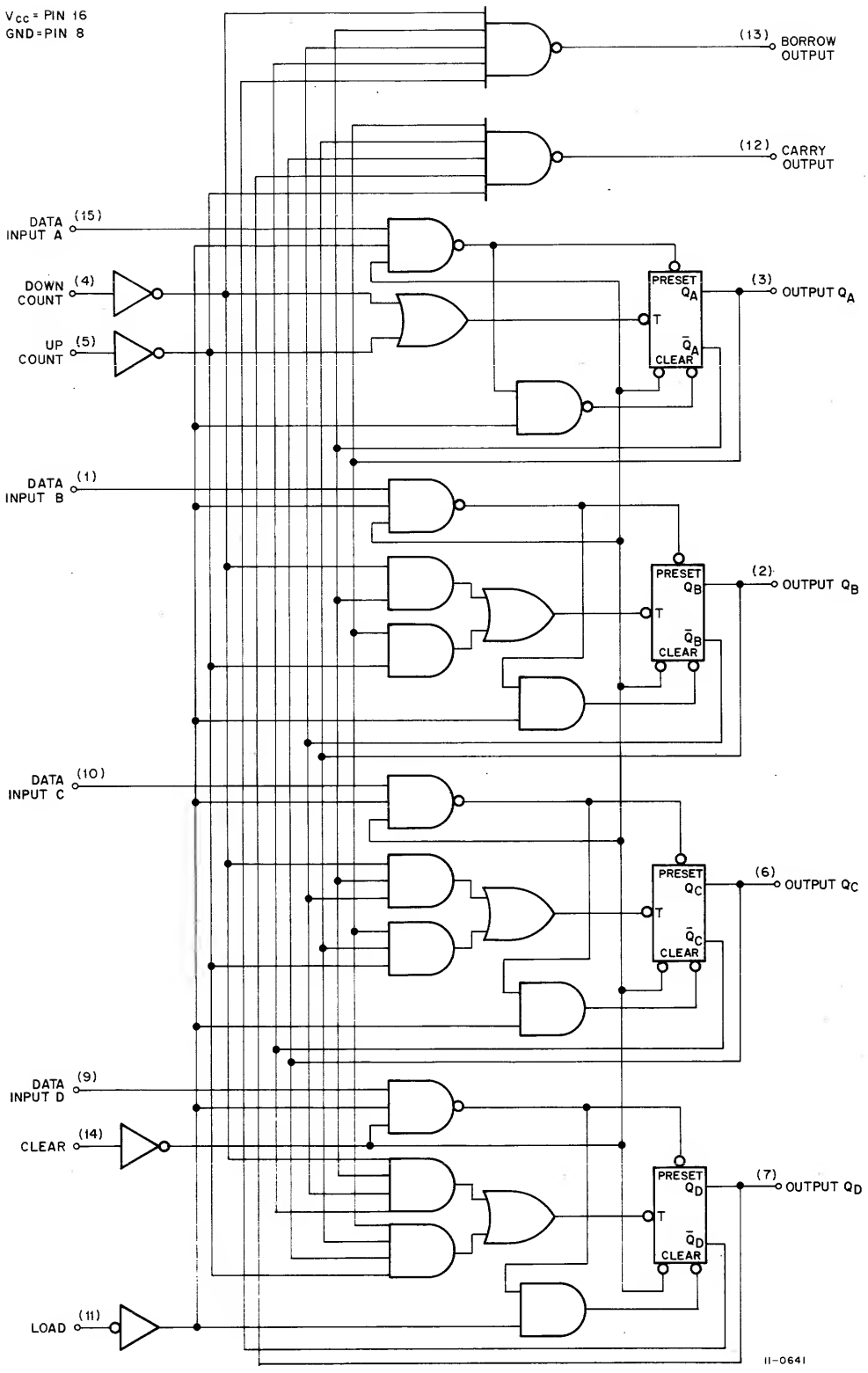
74175 Diagram

C.28 74193 SYNCHRONOUS 4-BIT UP/DOWN COUNTER (DUAL CLOCK WITH CLEAR)

The 74193 is incremented or decremented by a low to high level transition at the appropriate clock input while the other is held high. The outputs can be preset by applying the desired information to the data inputs with the load input low. A high on the clear input forces all outputs low. The borrow and carry outputs allow the counters to be cascaded.

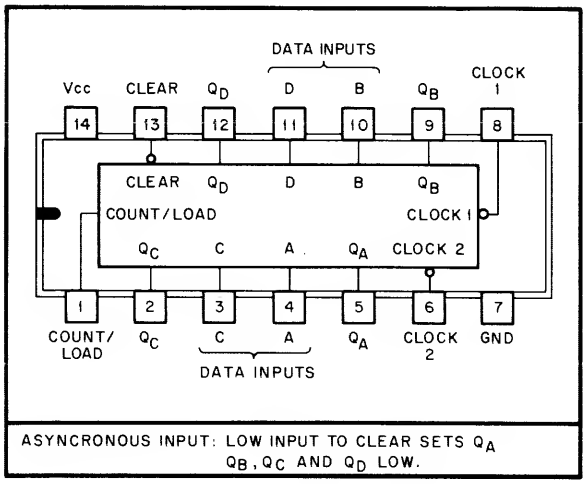


11-0640


V_{CC} = PIN 16
GND = PIN 8
(13) BORROW OUTPUT
(12) CARRY OUTPUT
DATA INPUT A (15)
DOWN COUNT (4)
UP COUNT (5)
DATA INPUT B (1)
DATA INPUT C (10)
DATA INPUT D (9)
CLEAR (14)
LOAD (11)
PRESET Q_A
T
$\bar{Q}_A$
CLEAR
(3) OUTPUT Q_A
PRESET Q_B
T
$\bar{Q}_B$
CLEAR
(2) OUTPUT Q_B
PRESET Q_C
T
$\bar{Q}_C$
CLEAR
(6) OUTPUT Q_C
PRESET Q_D
T
$\bar{Q}_D$
CLEAR
(7) OUTPUT Q_D
11-0641

C.29 74197 50-MHz PRESETTABLE DECODE AND BINARY COUNTERS/LATCHES

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE
(TOP VIEW)*



ASYNCRONOUS INPUT: LOW INPUT TO CLEAR SETS Q_A Q_B, Q_C AND Q_D LOW.

*Pin assignments for these circuits are the same for all packages.

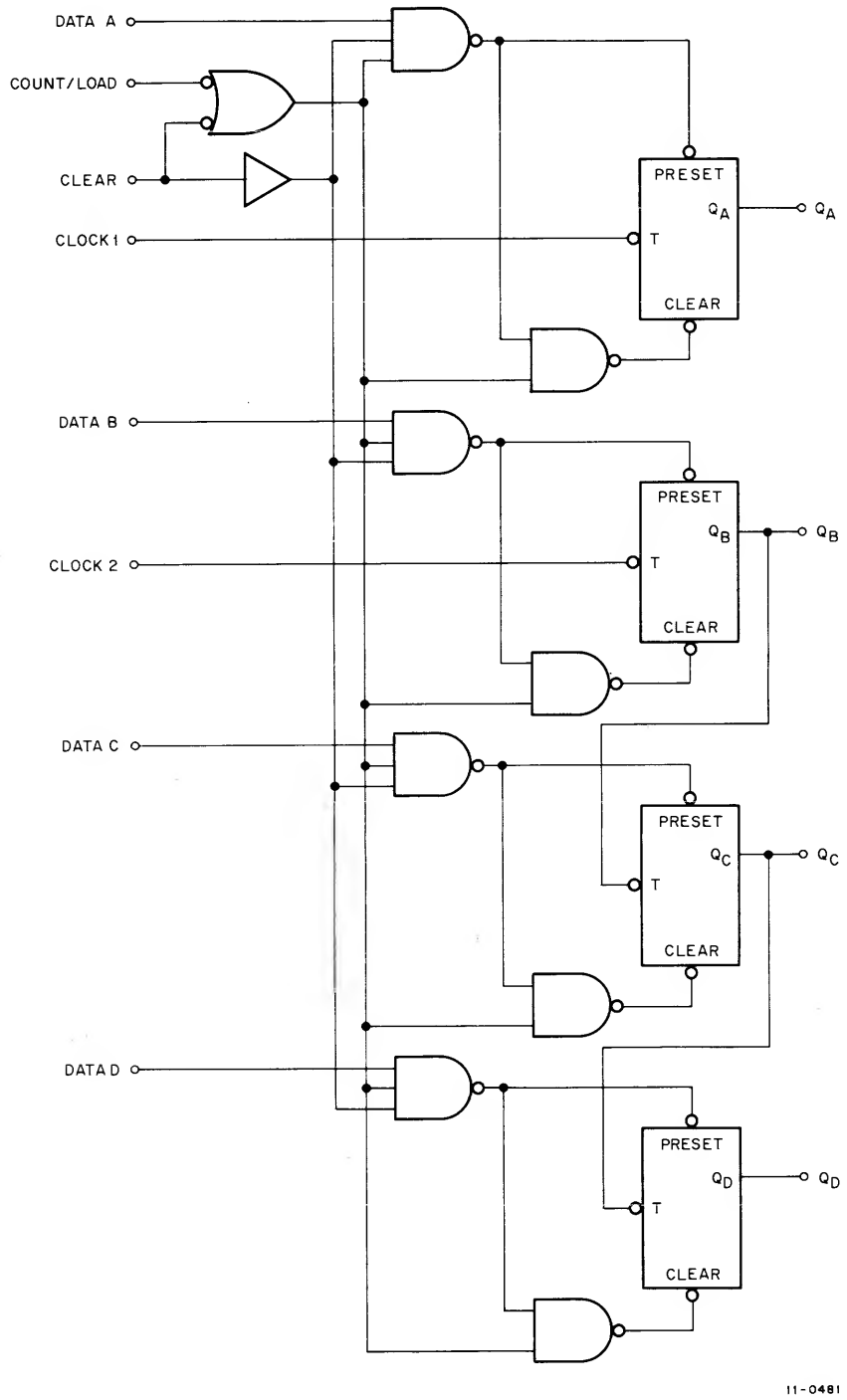
11-0482

74197 TRUTH TABLE

(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.


DATA A
COUNT/LOAD
CLEAR
CLOCK 1
DATA B
CLOCK 2
DATA C
DATA D
PRESET
Q_A
T
CLEAR
Q_A
PRESET
Q_B
T
CLEAR
Q_B
PRESET
Q_C
T
CLEAR
Q_C
PRESET
Q_D
T
CLEAR
Q_D
11-0481

APPENDIX D
UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

D.1 INTRODUCTION

This appendix provides a functional description of the UART. It includes a table of UART signal functions and simplified block diagrams and timing diagrams of the UART receiver and transmitter.

D.2 UART FUNCTIONAL DESCRIPTION

The UART is a MOS/LSI device packaged in a 40-pin DIP. It is a complete subsystem that transmits and receives asynchronous data in duplex or half duplex operation. The receiver and transmitter can operate simultaneously. The transmitter accepts parallel binary characters and converts them to a serial asynchronous output.

The receiver accepts serial asynchronous binary characters and converts them to a parallel output. The receiver and transmitter clocks are separate and must be 16 times the desired Baud rate. The allowable clock rate is DC to 160 kHz.

Control bits are provided to select: character length of 5, 6, 7, or 8 bits, (excluding parity) mode, odd or even parity, and one or two stop bits for 6, 7, or 8-bit characters. For 5-bit characters, 1 or 1-1/2 start bits are used. The format of a typical input/output serial word is shown in Figure D-1.

Both the receiver and transmitter have double character buffering so that at least one complete character is always available. A register is also provided to store control information.

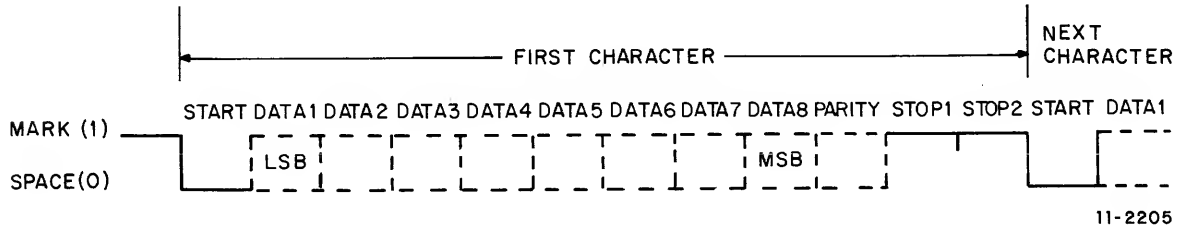


Figure D-1 Format of Typical Input/Output Serial Character

A block diagram and simplified timing diagram for the UART transmitter are shown in Figure D-2. The transmitter data buffer (holding) register can be loaded with a character when the TBMT (Transmitter Buffer Empty) line goes high. Loading is accomplished by generating a short negative pulse on the DS (Data Strobe) line. The positive-going trailing edge of the DS pulse performs the load operation. The character is automatically transferred to the UART transmitter Shift Register when this register becomes empty. The desired start, stop and parity bits are added to the data and transmission begins. One sixteenth of a bit time before a complete character (included stop bits) has been transmitted, the EOC (End of Character) line goes high and remains in this state until transmission of a new character begins.

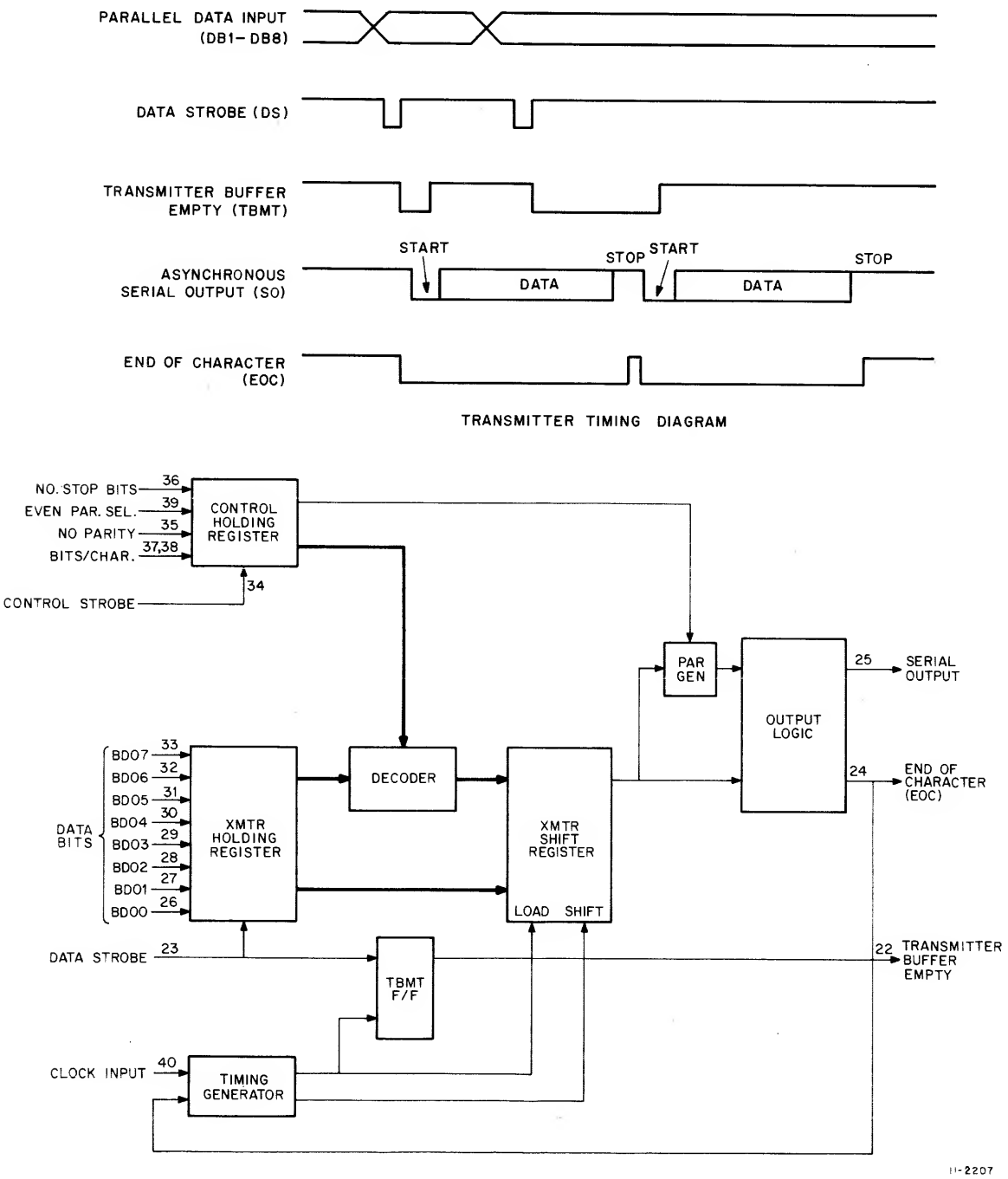
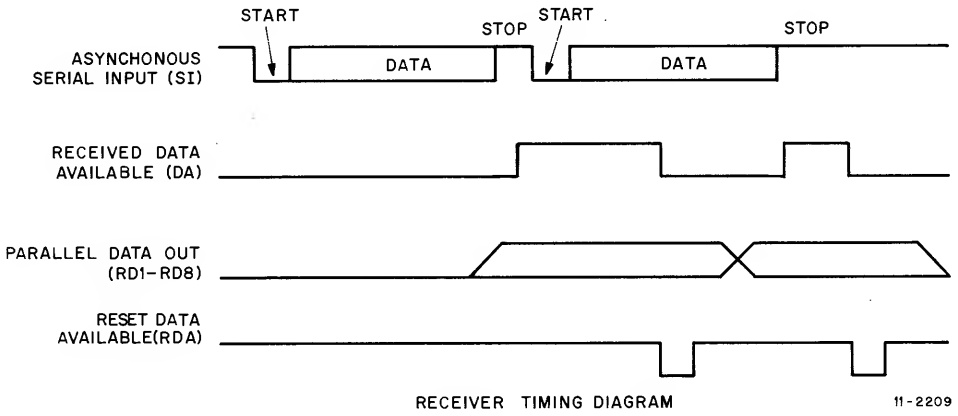


Figure D-2 UART Transmitter, Block Diagram and Simplified Timing Diagram

A block diagram and simplified timing diagram for the UART receiver are shown in Figure D-3. Serial asynchronous data is sent to the SI (Serial Input) line. The UART searches for a high to low (mark to space) transition on the SI line. If this transition is detected, the receiver looks for the center of the start bit as the first sampling point. If this point is low (space), the signal is assumed to be a valid start bit and sampling continues at the center of the subsequent data and stop bits. The character is assembled bit by bit in the receiver Shift Register in accordance with the control signals that determine the number of data bits and stop bits and the type of parity, if selected. If parity is selected and does not check, the PER (Receive Parity Error) line goes high. If the first stop bit is low, the FER (Framing Error) line goes high. After the stop bit is sampled, the receiver transfers in parallel the contents of the receiver Shift Register into the receiver data buffer (holding) register. The receiver then sets the DA (Received Data Available) line and transfers the state of the framing error and parity error to the Status Holding Register. When the DH11 accepts the receiver output, it drives the RDA (Reset Data Available) line low which clears the DA line. If this line is not reset before a new character is transferred to the receiver Holding Register, the OR (Overrun) line goes high and is held there until the next character is loaded into the receiver Holding Register.



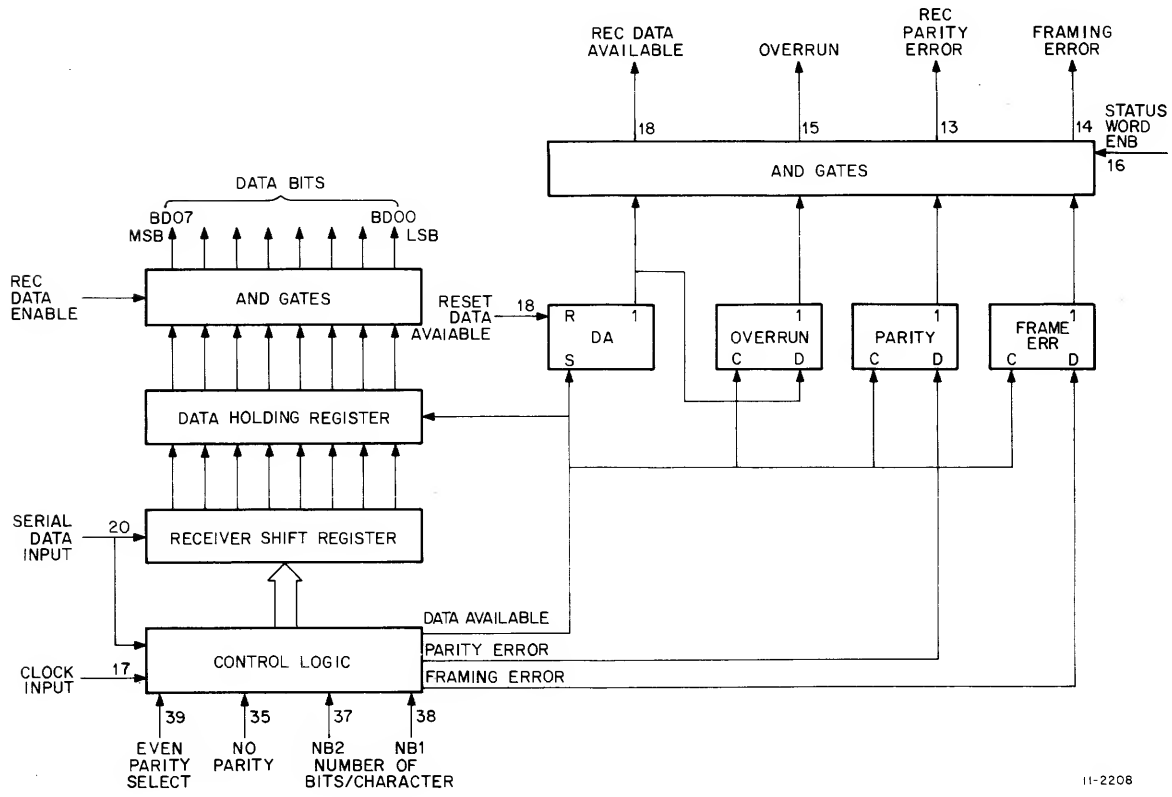


Figure D-3 UART Receiver, Block Diagram and Simplified Timing Diagram

Figure D-4 is a pin/signal designation diagram for the UART. The function of each signal is given in Table D-1. In the Function column, the references to high and low signals are with respect to the pins on the UART. This information is used during servicing of the device. Programmers should refer to the DH11 register descriptions (Chapter 3) for information concerning the function of these signals.

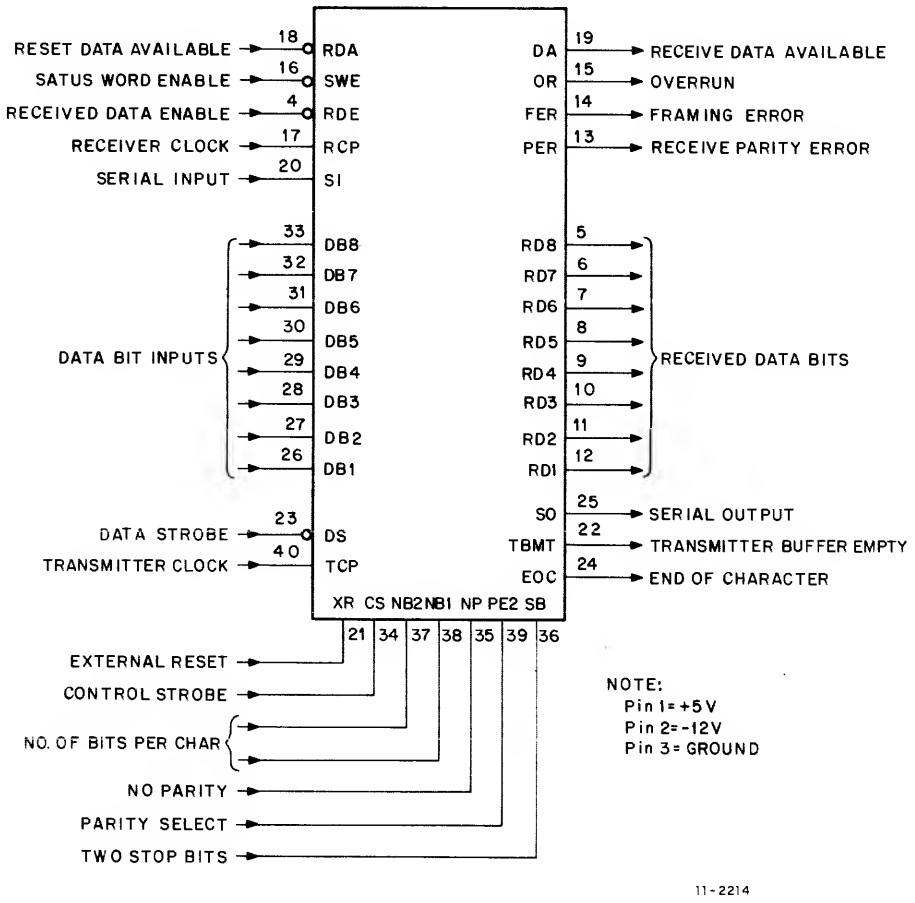


Figure D-4 UART Signal/Pin Designations

Table D-1
UART Signal Functions

Pin No.	Mnemonic	Name	Function
5-12	RD1-RD8	Received Data	Eight data out lines that can be wire ORed. RD8 (pin 5) is the MSB and RD1 (pin 12) is the LSB. When 5, 6, or 7 bit character is selected, the most significant unused bits are low. Character is right justified into the least significant bits.
13	PER	Receive Parity Error	Goes high if the received character parity does not agree with the selected parity.
14	FER	Framing Error	Goes high if the received character has no valid stop bit.
15	OR	Overrun	Goes high if the previously received character is not read (DA line not reset) before the present character is transferred to the receiver Holding Register.
16	SWE	Status Word Enable	When low, places the status word bits (PE, OR, TBMT, FE, and DA) on the output lines.
17	RCP	Receiver Clock	Input for an external clock whose frequency must be 16 times the desired receiver Baud rate.
18	RDA	Reset Data Available	When low, resets the received DA (Data Available) line.
19	DA	Received Data Available	Goes high when an entire character has been received and transferred to the receiver Holding Register.
20	SI	Serial Input	Input for serial asynchronous data.
21	XR	External Reset	After power is turned on, this line should be pulsed high which resets all registers, sets serial output line high, sets end of character line high, and sets transmitter buffer empty line high.
22	TBMT	Transmitter Buffer Empty	Goes high when the transmitter Data Holding Register may be loaded with another character.
23	DS	Data Strobe	Pulsed low to load the data bits into the transmitter Data Holding Register during the positive-going trailing edge of the pulse.
24	EOC	End of Character	Goes high each time a full character, including stop bits, is transmitted. It remains high until transmission of the next character starts. This is defined as the mark (high) to space (low) transition of the start bit. This line remains high when no data is being transmitted. When full speed transmission occurs, this lead goes high for 1/16 bit time at the end of each character.

Table D-1 (Cont)
UART Signal Functions

Pin No.	Mnemonic	Name	Function
25	SO	Serial Output	Output for transmitted character in serial asynchronous format. A mark is high and a space is low. Remains high when no data is being transmitted.
26-33	DB1-DB8	Data Input	Eight parallel Data In lines. DB8 (pin 33) is the MSB and DB1 (pin 26) is the LSB. If 5, 6, or 7 bit characters are selected, the least significant bits are used.
34	CS	Control Strobe	When high, places the control bits (POE, NP, SB, NB1 and NB2) into the control bits Holding Register.
35	NP	No Parity	When high, eliminates the parity bit from the transmitted and received character and drives the received parity error (PER) line low. As a result, the receiver does not check parity on reception and during transmission the stop bits immediately follow the last data bit.
36	2 SB	Two Stop Bits	Selects the number of stop bits that immediately follow the parity bit. A low inserts 1 stop bit and a high inserts 2 stop bits.
37,38	NB2, NB1	Number of Bits per Character (Excluding Parity)	Select 5, 6, 7, or 8 data bits per character as follows. **Bits/ Char** — **NB2 (37)** — **NB1 (38)** 5 — L — L 6 — L — H 7 — H — L 8 — H — H
39	POE	Even Parity Select	Selects the type of parity to be added during transmission and checked during reception. A low selects odd parity and a high selects even parity.
40	TCP	Transmitter Clock	Input for an external clock whose frequency must be 16 times the desire transmitter Baud rate.

APPENDIX E
DH11-AD MODEM CONTROL INTERFACE

E.1 GENERAL DESCRIPTION

The DH11-AD modem control unit is comprised of the M7807 and M7808 module sets (Figure E-1). It is used to interface the modem control signals between the modem and processor. Data is handled by the DH11-AD asynchronous 16-line multiplexer. The modem control unit multiplexes 16 asynchronous modem interfaces. The unit provides necessary control signals and levels to interface with Bell 103A/E/F/G/H, 202C/D, and 811B modems or their equivalents. The interface levels are EIA/CCITT compatible for data set operations. Table E-1 is a glossary of modem control terms.

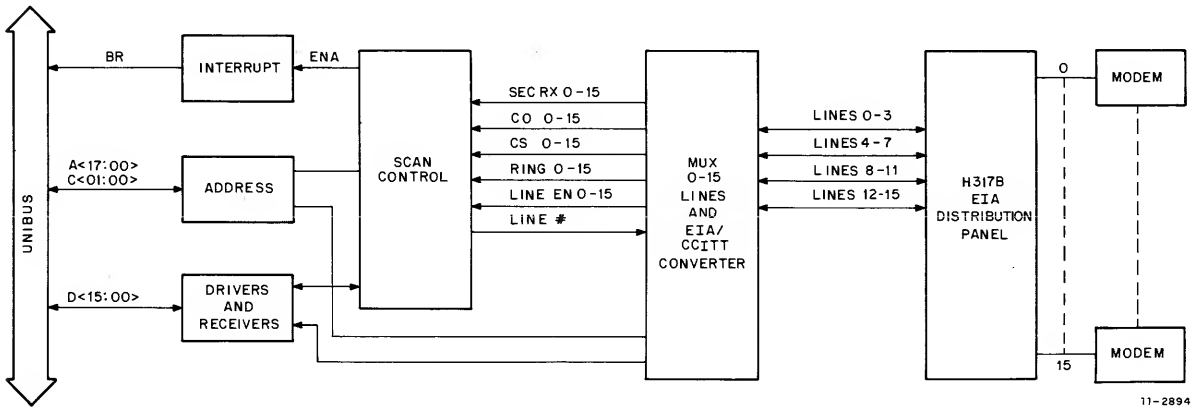


Figure E-1 Modem Control Block Diagram

E.2 FUNCTIONAL DESCRIPTION

The modem control signals for up to 16 lines are connected to the M7807 and M7808 through the H317B EIA distribution panels. Level conversion for all lines is provided by these modules.

The modem control unit scans the SEC RX, CLEAR TO SEND, CARRIER, and RING lines for each modem line sequenced by a line counter in the logic. When a transition is detected on a line, for the modem line selected by the line counter, an interrupt condition is generated. If interrupt enable and line enabled are both true, the interrupt request logic asks for control of the Unibus. Likewise, the address selection logic allows the processor to send SEC TX, REQUEST TO SEND, and TERMINAL READY to the modem designated by the line counter. The line counter enables the particular signal to be asserted on the line designated. The line counter is sequenced through the ring counter, which is clocked internally and enabled by the program controlled scan enable and step conditions.

Table E-1
Glossary

Modem Control Terms	Definitions
TP	Test Point
SEC RX	Secondary Received Data (202)
CARRIER or CO	Received Line Signal Detector (CF)
CS	Clear to Send (CB)
RING	Ring Indicator (CE)
LINE CNT	Line Count
CNTR	Counter
LSB	Least Significant Bit
MSB	Most Significant Bit
EN	Enable
INI	Initialize
INTR	Interrupt
HOLD (Ring, CO, CS, SEC RX)	Holding register for last known status (not current)
REQUEST TO SEND or RS	Request to Send (CA)
SEC TX	Secondary Transmitted Data (202)
TERM RDY	Data Terminal Ready (CD)
LINE EN	Line Enable
X DCDR	X Decoder for Memory
Y DCDR	Y Decoder for Memory
BUSY	Force Busy (103E)

There are two basic types of modem control: Transmit (to the modem) and receive (from the modem). The transmit control functions are: Terminal Ready, Request to Send, and Secondary Transmit. The receive control functions are: Clear to Send, Carrier, Secondary Receive, and Ring. The sequential usage of these control leads for the various modems can be determined by using the modem timing diagrams shown in Appendix F. For example, a typical channel establishment sequence for the 103A modem would be as follows:

a. 103A originate mode channel establishment (Figure F-1, Appendix F).

   1. Setting the Data Terminal Ready lead to 1, followed by dialing via the DN11 Automatic Dialing Unit or by manual means initiates a call to the remote modem.

   2. When the data link is established by the remote modem answering the call, Carrier Detect and Clear to Send make the transition to the ON state.

   3. If the modem control's Line Enable for the line is set and Interrupt Enable and Scan Enable are set, the transitions of Carrier and Clear To Send are detected and an interrupt is generated to the Unibus.

   4. At this time, the DH11-AD may transmit and/or receive data over the established data communications link.

b. 103A answer mode channel establishment (Figure F-1, Appendix F). Line Enable, Scan Enable, and Interrupt Enable are assumed true.

   1. A Ring signal is forwarded from the modem to the modem control. This OFF to ON transition is detected by the scanner and forwarded to the Unibus as an interrupt condition.

2. The data link may then be established with the calling modem or line by setting Data Terminal Ready.

3. When the transitions of Carrier and Clear To Send occur (OFF to ON), the communications data link is established and an interrupt condition is presented to the Unibus.

4. The DH11-AD may now transmit and/or receive data.

E.3 PHYSICAL DESCRIPTION

Modem control occupies two system unit module slots (1/2 system unit) in the DH11-AD (Figure E-2). This scan-operated modem control for 16 asynchronous modems, uses the following parts:

Quantity	Part	Description
1	M7808	Data MUX (8 Lines), Scan Control
1	M7807	Data MUX (8 Lines) Address Selector Interrupt Control
4	BC08R-12	Mylar Cable (4 Lines)
1	H861	Test Connector (16 Lines)
1	H315	Modem Test Connector

The interconnection of the parts is shown in Figure E-2. The cabling for the modem level converters is part of the modem control.

E.4 ENVIRONMENTAL LIMITS, PERFORMANCE SPECIFICATIONS, AND INTERFACE SPECIFICATIONS

The environmental limits, performance specifications, and interface specifications are listed in Table E-2.

E.5 DETAILED DESCRIPTION

E.5.1 Introduction

The modem control consists of four basic logic units. They are the Address Selector Logic, Interrupt Control Logic, Scan Logic, and the Data Multiplexer Logic (MUX). These units are discussed in detail in the following paragraphs. Refer to Figure E-3 for the functional scan block diagram. Also, the maintenance mode of operation is discussed.

E.5.2 Address Selector Logic

The address selector logic (M7807) is jumper-prepared to recognize the two register addresses assigned to the modem control. When the bus designates either of these addresses, they are recognized by the selector logic and, according to the bus operation (DATO, DATI, DATIP, or DATOB), SELECT, IN and OUT signals are generated. DATI or DATIP bus operations designate the IN selection signal for gating to the bus; DATO or DATOB designate the OUT selection signal for gating from the bus. SELECT 0 and OUT LOW load the CSR, while SELECT 0 and IN gate the CSR to the bus. SELECT 2 and IN gate the MUX TERM RDY, MUX LINE EN, MUX RQ TO SEND, and MUX SEC TX to the bus along with MUX SEC RX, MUX CLEAR TO SEND, MUX CARRIER, and MUX RING. Signals SELECT 2 and OUT LOW enable the generation of the clock for MUX transmitting to the modem lines.

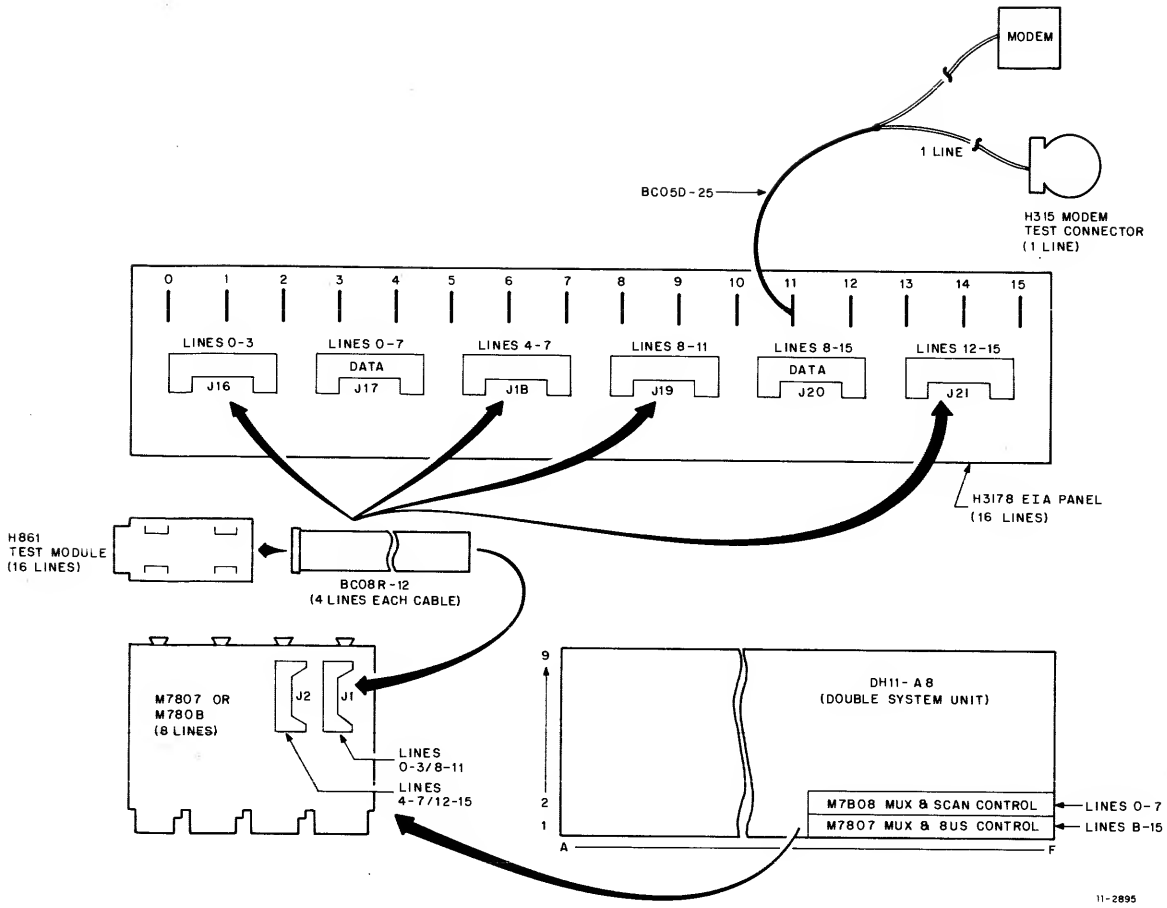


Figure E-2 Modem Control Hardware Configuration

E.5.3 Interrupt Control Logic

The M7807 Interrupt Control logic enables the unit to gain control of the bus (become bus master) and perform an interrupt operation. This is accomplished through a bus request (BR) at BR level 4. Detection of a transition in CARRIER, SEC RX, CLEAR TO SEND, or RING signal lines from any modem, designated by the modem line counter, generates an interrupt request through the interrupt logic as long as INTR EN has been set by the program. Any of these conditions causes the interrupt control to generate the BR to the processor requesting bus control.

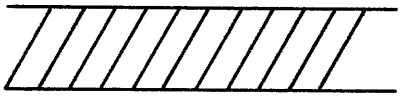
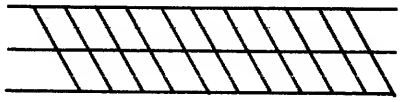
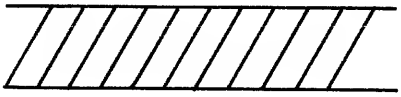
E.5.4 Scan Logic

The scan logic (engineering drawing D-CS-M7808-0-1, sheets 2 and 3) includes the control logic for the modem control and the Unibus receivers and drivers. The Unibus receivers and drivers are standard for the PDP-11 and meet all requirements for connection to the Unibus. The control logic performs the programmable functional conditions of the CSR. The principal logic units of the scan logic are the ring counter, line counter, scan memory logic, and the interrupt logic.

Table E-2
Specifications

Environmental Limits	
Power requirements	+5 V, 2.4 A
Temperature	10° C to 50° C
Humidity (relative)	Up to 90% (non-condensing)
Performance Specifications	
Interrupts	CARRIER, SEC RX, CLEAR TO SEND, and RING transitions cause interrupts.
Modem status maximum rate change	10,000 Hz for both receive and transmit circuits.
Scan rate	Tests line conditions for interrupts at a rate of 1 MHz ± 10% or one line per 1.2 μs, approximately.
Scan control	Programmable to allow scan to run free (SCAN EN) or to sequentially step through Scan line by line (STEP).
LINE counter	Line numbers (LINE #) may be accessed by program sequentially or randomly, without concern for internal synchronization.
Scan limitations	The Scan cannot be halted and the line number changed with one instruction due to the Read/Write cycles of the Scan's memory. Also, the program must wait for CLR SCAN (programmable) to ripple through the control memory logic.
Interrupt bus request	Hard-wired to level 4 (BR4).
Interface Specifications	
Unibus	Presents one unit load to the bus and meets all Unibus electrical specifications.
Modem interface	Provides modem control leads compatible to modem types 103A, 103F, 103E (G and H), 202C/D, and 811B. (Types may be mixed over the 16 lines available.) These lines are EIA RS-232-C and CCITT compatible.
Condensed EIA RS-232-C Electrical Specifications	
Driver output logic levels with 3K to 7K load	$15\ V > _{oh} > 5\ V$ $-5\ V > _{ol} > -15\ V$
Driver output voltage with open circuit	$/V_o/ < 25\ V$
Driver output impedance with power off	$20 > 300$ ohms

Table E-2 (Cont)
Specifications

Condensed EIA RS-232-C Electrical Specifications (Cont)	
Output short circuit current	$/I_o/ < 0.5$ A
Driver slew rate	$\frac{dv}{dt} < 30$ V μs
Receiver input impedance	$7\ k\Omega > R_{in} > 3\ k\Omega$
Receiver input voltage	±15 V compatible with driver
Receiver output with open circuit input	Mark
Receiver output with +3 V input	Space
Receiver output with −3 V input	Mark
+15 +5 	LOGIC "0" = SPACE – CONTROL ON
	Noise margin
+3 0 −3 	Transition region
	Noise margin
−5 −15 	LOGIC "1" = MARK = CONTROL OFF

Initiation of the modem control is achieved through the program-controlled device registers. Initialization is achieved through the CLR SCAN signal from the program and BUS INITIALIZE. These signals combine to clear the logic flip-flops and counters, while setting CLEAR CYCLE. Signal CLEAR CYCLE puts a low to the direct clear inputs of the HOLD flip-flops (SEC RX HOLD, CS HOLD, CO HOLD, and RING HOLD) and inhibits inputs from the MUX to scan memory while the memory is being cycled through all lines. The CLEAR CYCLE flip-flop is then cleared when all scan memory locations have been written with 0s. The modem control is now initiated by setting the SCAN EN bit. SCAN EN with DONE clear (no interrupt conditions present) inputs the 8271 Ring Counter. The CLOCK cycles the ring counter through four states; that is, the ring counter increments the LINE CNTR (LINE INCR), loads the HOLD flip-flops with the last known contents of memory (at LINE #) (LD HOLD), transfers the current status of the LINE # to the memory section (IN WRITE), and tests the contents of the HOLD flip-flops and the memory section (at LINE #) for interrupt-causing conditions (INTR TEST). This four-state ring counter sequence is repeated for each line (LINE #), sequentially, as long as the SCAN EN condition with DONE clear is present to the ring counter. The programmable flip-flop STEP can also enable the ring counter, but for only one count; STEP enables one clock of the ring counter to increment the LINE CNTR (LINE INCR) which feeds back to clear STEP. The ring counter sequences the other three steps (LD HOLD, IN WRITE, and INTR TEST) before coming to rest.

The LINE CNTR is programmable for loading with a desired line count from the bus (BUS DATA 00 through BUS DATA 03). The LINE CNTR outputs provide line selection for testing, sensing, and modifying the line status on a per line basis. The LINE CNTR output also inputs the memory to select the memory locations in the 7489 for each line's SEC RX, CS, CO, and RING status. When the ring counter sequences the WRITE IN signal, the status of each

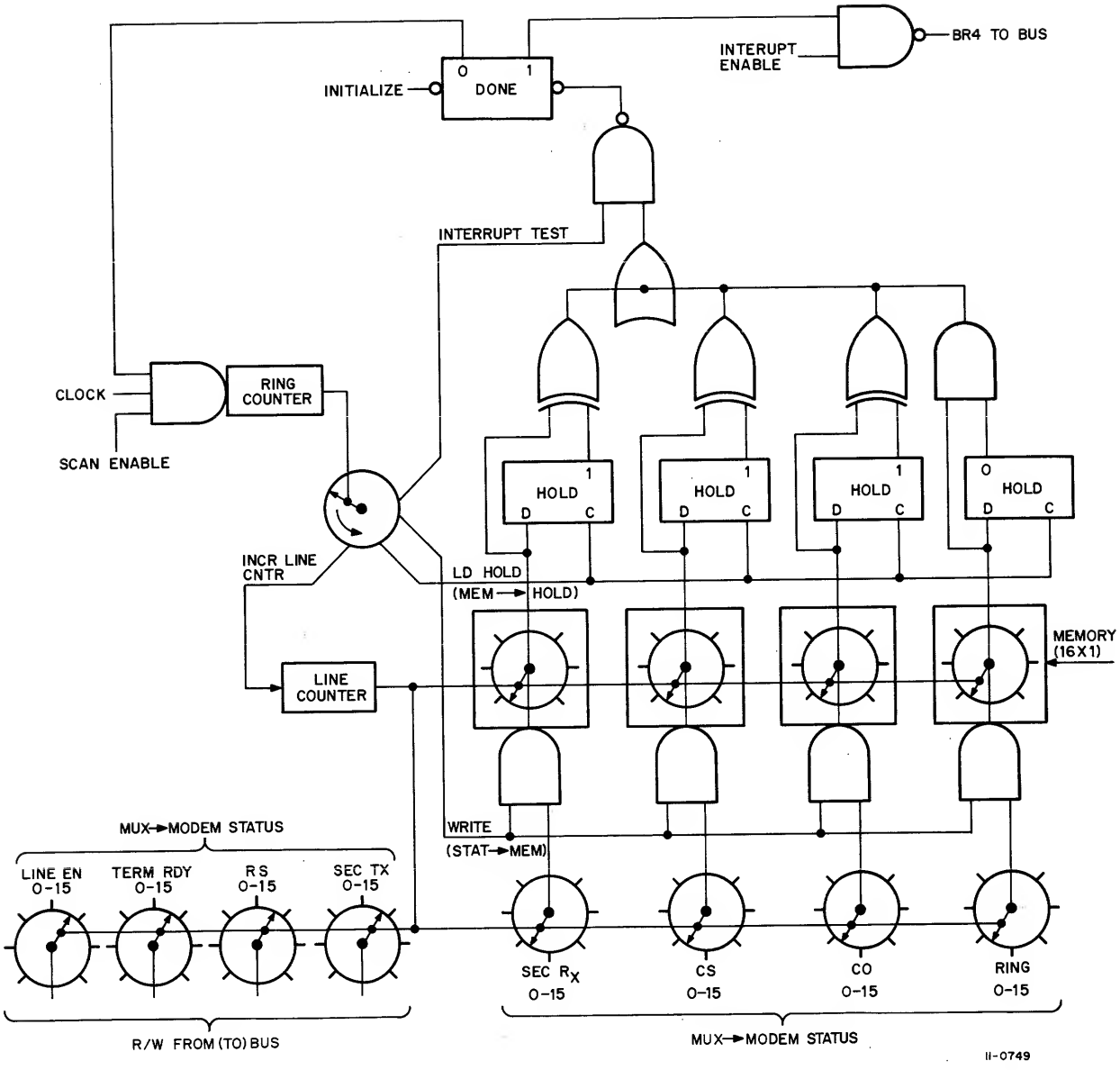


Figure E-3 Scan Functional Block Diagram

of the RING, CARRIER, SEC RX, and CLEAR TO SEND lines for the particular modem (LINE #) is loaded into the memory location of the 7489s designated by the LINE CNTR inputs.

During INITIALIZE, when the X- and Y-decoders are loaded from LINE 0000, the decoder's LSB (least significant bit) output combines with the ring counter WRITE IN sequence signal to clear the CLEAR CYCLE flip-flop. The HOLD flip-flops can now be input from the 7489 memory. For each line selected through the X- and Y-decoders, the states of the MUX SEC RX, MUX CLEAR TO SEND, MUX CARRIER, and MUX RING are loaded into the respective memory locations by the WRITE IN signal from the ring counter. When WRITE IN is unasserted, the memory presents the state for the respective LINE # to HOLD flip-flops. Each time the ring counter sequences LD HOLD for each line, the HOLD flip-flops are loaded with the contents of the respective memory locations. The memory contents are the last known state or status designated by the LINE CNTR. When the ring counter sequences WRITE IN, the new status is loaded into memory for the particular line. This new status (SEC RX, CLEAR TO

SEND, CARRIER, and RING) is then compared with the contents of the respective HOLD flip-flops in the Exclusive OR gates for SEC RX, CLEAR TO SEND, and CARRIER and the AND gate for RING. This gating operation detects transitions in the line status each time the LINE # is sequenced. A (low to high) transition of any of the conditions for a particular line generates an interrupt condition. A (high to low) transition also generates an interrupt condition for all lines except RING which is compared to the previous line state by an AND gate. This is tested when the ring counter sequences INTR TEST. The presence of an interrupt condition at INTR TEST with the MUX LINE EN present (see MUX description) sets DONE. DONE set, with INTR EN set by the program, generates an interrupt condition to the interrupt control logic, which generates a bus request to the processor. An interrupt will not occur if the program has modified the LINE CNTR and the ring counter has not cycled. For example, if the Scan last tested LINE #5, followed by the program's modification of the LINE CNTR to LINE #8, for example, the HOLD flip-flops now contain the line status of LINE #5, while the memory is at LINE #8 and inputting the transition gates for LINE #8. Therefore, any transitions detected are a function of LINE #5 and LINE #8 and are not valid interrupt conditions.

E.5.5 Modem Control (MUX) Logic

The modem control (MUX) logic contains the status selector logic for each line interfaced (engineering drawing D-CS-7808-0-1). The status to the modem is Read/Write and the status from the modem is Read Only. Read/Write status control signals are LINE EN, TERM RDY, RQ TO SEND, and SEC TX. The Read Only status control signals are RING, CARRIER, CLEAR TO SEND, and SEC RX. For any Read Only status to be read, the respective LINE EN must be on. If this is not the case, RING, CARRIER, CLEAR TO SEND, and SEC RX are blinded to the line status from the scan control logic.

The MUX Write is clocked by the LINE DCDR. The LINE DCDR is input with the LINE CNTR output and WRITE SEL. WRITE SEL is initiated by the selection logic through OUT LOW and SELECT 2, and thus program-controlled. Also, WRITE SEL reflects the LINE CTR GROUP 0–7 or GROUP 8–15 signals that enable the respective LINE DCDR of each MUX module. The LINE DCDR provides a CLOCK signal for each line's status signal selector. Each CLOCK for each line inputs a respective 74175 for clocking in LINE EN and either SEC TX, TERM RDY, or RQ TO SEND to be transmitted on the respective modem line. The data bits for LINE EN, SEC TX, TERM RDY, and RQ TO SEND input the 74175 from the receivers (D00 to D03). CLOCK enables the 74175s to output to the respective modem lines.

Three of the LINE CNTR outputs provide enabling signals for the 74151 selectors in the MUX. The states of these inputs according to the LINE # select the proper line to be enabled at the selectors from the respective modem lines. For the signals coming from the modems, the RING SELECTOR, CARRIER SELECTOR, CLEAR TO SEND SELECTOR, and SEC RX SELECTOR are enabled at the current LINE # by INTR STATUS. INTR STATUS is asserted to enable the receiver selectors when CLEAR CYCLE is not set and MUX LINE EN is present. The receiver selectors output MUX RING, MUX CARRIER, MUX CLEAR TO SEND, and MUX SEC RX to the memory section of the scan logic to test for interrupts. MUX LINE EN is generated in the transmit selector when the programmable LINE EN is set for the respective LINE #, enabling the selector from the LINE CNTR. These transmit selectors are enabled by R/W STATUS, which asserts to the respective MUX module for either Lines 0–7 (GROUP 0–7, from LINE CNTR) or Lines 8–15 (GROUP 8–15 from the LINE CNTR). The control signal status conditions are available to the program with the receive conditions handled by the scan logic for interrupt conditions and the transmit conditions for each line sent to the respective modems.

E.5.6 Maintenance Mode

The maintenance mode of operation in the modem control is achieved by the programmed setting of the MAINT MODE flip-flop of the CSR. Setting MAINT MODE forces MUX SEC RX, MUX CLEAR TO SEND, MUX CARRIER, and MUX RING low, asserting a transition for the line designated by the line counter. These conditions can then be checked by the program through the CSR and allowed to cause interrupt conditions.

E.6 OPERATIONAL PROGRAMMING

The two programmable device registers and their specific bit assignments are listed in the following paragraphs.

E.6.1 Control Status Register (CSR) (Address: 770XX0)

Bit	Status	Description
03:00	LINE #	The LINE # bits are the binary addresses for the 16 lines (0–15) as follows: **Bit 3 2 1 0 — Line #** 0 0 0 0 — 0 0 0 0 1 — 1 . . . 1 1 1 1 — 15 If the Scan is cleared by INITIALIZE or CLR SCAN, the Line # Register will settle in 16 μs ± 10%. When settled, the Line # Register will be set to Line # 0 (0000). **NOTE** **When the Scan is enabled (or STEP) the next line to be tested will always be Line # +1. These bits are Read/Write and are cleared by INITIALIZE and by CLR SCAN.**
04	BUSY	BUSY provides a program indicator that is set to 1 when the Scan is cycling. This bit is particularly useful to determine when a CLR SCAN (bit 11) has completed the task of cycling 0s into the Scanner's memory elements. In addition, this bit *must* be tested for 0 if SCAN ENABLE was turned off preparatory to changing the Line #. In Interrupt Mode, this procedure guarantees that detected transitions are serviced before the Line # is changed. (If functioning with interrupts OFF, then DONE should be tested after BUSY is found to be 0.)
05	SCAN EN	The SCAN ENABLE flip-flop allows the scan to "free run," i.e., testing all lines sequentially if the DONE flip-flop is cleared. When the SCAN EN flip-flop is set to 1 and DONE is 0, a ring counter is allowed to cycle in the following order (from Rest): a. Increment line counter. b. Store contents of memory (Line # Address) in the HOLD flip-flop. c. Write current modem status into memory. d. Compare HOLD and contents of memory for Interrupt conditions.

Bit	Status	Description
05 (Cont)		The ring counter continues to cycle (a to d) if DONE remains 0 and SCAN EN is set. If the SCAN EN flip-flop is negated while the ring counter is cycling (i.e., DONE not set) the ring counter will come to rest in 1.2 μs ± 10% (MAX). The line # Register must not be changed until BUSY (bit 04) is found to be 0. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
06	INTR EN	If set to 1, Interrupt Enable allows DONE to cause an interrupt on priority four. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
07	DONE	The DONE flag, when set to 1, indicates that the hardware Scan has detected a transition on CARRIER, SEC RX, CS, or the RING Modem Status leads. Additionally, DONE freezes the Scan which makes the following available to the programmer: a. The Line # that caused the interrupt b. The state of the flags (4 bits) c. Modem status (8 bits) This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
08	STEP	STEP, when set to 1, causes the Scan to increment the Line # and test that line for interrupts causing transitions. STEP can be used in place of SCAN EN, but care should be exercised that the Scan rate is great enough (milliseconds) so that double carrier transitions will be detected. Additionally, DONE does not inhibit STEP. A STEP requires 1.2 μs ± 10% to execute. This bit is Write 1s only.
09	MAINT MODE	When the MAINT MODE flip-flop is set to 1, it conditions the Scan Input (RING, CLEAR TO SEND, CARRIER, and SEC RX) to a 1 or ON state. Utilizing STEP or SCAN EN with MAINT MODE exercises 100 percent of the scan logic (not the data multiplexers). This includes the interrupt circuits and the address selector. This mode provides a diagnostic feature as well as on-line test facility for the DM11-BB's interaction with the Unibus. This bit is Read/Write and cleared by INITIALIZE and CLR SCAN.
10	CLEAR MUX	CLEAR MUX clears the REQUEST TO SEND, TERMINAL READY, SEC TX, and LINE EN flip-flops for all lines, when this bit is set to 1. This bit is Write 1s only.
11	CLR SCAN	CLEAR SCAN clears all active functions (Line #, SCAN EN, etc.) and the memory logic when this bit is set to 1. The memory logic requires 18.8 μs ± 10% to cycle a CLEAR through the memory locations. This function is especially useful if the programmer requires knowledge of the ON states of CARRIER, CLEAR TO SEND, RING and SEC RX. When the Scan is enabled (or STEP) following a CLR SCAN, an interrupt will occur for all ON states as they will appear (to the logic) as OFF to ON transitions.

Bit	Status	Description
12	SEC RX	The SECONDARY RECEIVE flag is 1 if an ON to OFF or an OFF to ON transition has occurred on this modem lead. This bit is redefined as RESTRAINT when the 811B Modem is used. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.
13	CS	The CLEAR TO SEND flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED or CLR SCAN.
14	CO	The CARRIER flag is 1 if an ON to OFF or OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.
15	RING	The RING flag is 1 if an OFF to ON transition has occurred on this modem lead. This bit is not valid if the program has changed the LINE # and the Scan has not cycled for one or more lines. This bit is Read Only and presents 0 when INITIALIZED and CLR SCAN.

E.6.2 Line Status Register (LSR) (Address: 770XX2)

Bit	Status	Description
00	LINE EN	The LINE ENABLE flip-flop, when asserted, enables RING, CO, CS, and SEC RX to be sampled (line status) by the program, and to be tested for transitions. This bit is Read/Write and cleared by INITIALIZE and CLEAR MUX.
01	TERM RDY	Controls switching of the data communications equipment to the communication channel (via modem). Auto-Dial and Manual Call origination: Maintains the established call. Auto-Answer: Allows "handshaking" in response to a RING signal. This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.
02	RS	When REQUEST TO SEND is set to 1, it conditions the modem for transmit if the communications channel has been established (switched network). When the DM11-BB is used to interface with 103E (or equivalent) modems, this lead is redefined as FORCE BUSY (RS = 1 = FORCE BUSY "ON"). This bit is Read/Write and is cleared by INITIALIZE and CLEAR MUX.

Bit	Status	Description
03	SEC TX	The SECONDARY TRANSMIT (202) flip-flop, when 1, presents a MARK to the modem's secondary transmit lead. This bit is Read/Write and is cleared by INITIALIZE or CLEAR MUX.
04	SEC RX	The state of the modem's Secondary Receive lead, when 1, is a MARK state. The SEC RX bit is inhibited when the LINE EN flip-flop is 0. When the DM11-BB is used to interface with the 811B modem, this lead is redefined as RESTRAINT. This bit is Read Only.
05	CS	This bit reflects the current state of the modem CLEAR TO SEND lead. An ON indicates that the modem is ready to transmit data. This lead is most often the result of the REQUEST TO SEND lead. The CS bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.
06	CO	This bit reflects the current state of the modem carrier control lead. An OFF indicates that no signal is unsuitable for demodulation. The CO bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.
07	RING	This bit reflects the current state of the modem's ring lead. The RING bit is inhibited when the LINE EN flip-flop is 0. This bit is Read Only.
		NOTE **The Line Status Register bits 07:04 are inhibited when LINE EN is 0.**

E.6.3 System Addresses

Addresses are assigned for sixteen DH11-AD modem controls per system and are assigned as follows:

1st control	Address	770500
		770502
2nd control	Address	770510
		770512
.		.
.		.
.		.
16th control	Address	770670
		770672

E.6.4 Interrupt Vectors

Each control requires one interrupt vector. The vector addresses are assigned upward from 300 to 777. The modem control falls in behind the DN11 in contiguous assignments from 300. The sequential list leading to the modem control is:

DC11
KL11
DP11
DM11-AA
DN11
DM11-BB or DH11-AD modem control

The DM11-BB option and the DH11-AD's modem control module set share the same address and vector space. Both may be in a single system since they are software compatible.

E.6.5 Timing Considerations

The control's timing considerations consist of scan control and CLR SCAN operations. Scan control through the CSR allows the scan to either run free (SCAN EN) or to be sequentially stepped through the line counter line by line (STEP bit of CSR). The Read/Write cycles of the scan logic force the program to wait after issuing CLR SCAN, until it has cycled through the memories. Also, the scan's Read/Write cycles prevent halting the scan and changing the line number with one machine cycle.

E.7 MAINTENANCE

E.7.1 Introduction

Maintenance consists of running two diagnostic software tests: the ON LINE and OFF LINE tests. The ON LINE diagnostic tests 100 percent of the scan logic, interrupts, and the Unibus interface. Additionally, 70 percent of the data multiplexer may be tested. The OFF LINE test uses a test connector to test 100 percent of the modem control, up to the point of demarcation at the modem interface. Paragraph E.7 provides instructions for running the tests as well as the hardware configurations for the respective tests.

E.7.2 Testing Configurations

The test/diagnostic procedures provide for four test configurations, two for the OFF LINE and two for the ON LINE tests are as listed:

OFF LINE (used for production test and acceptance)

a. Modem control with H861 termination

b. Modem control terminated with H315

ON LINE (limited data flow)

a. Modem loop back configuration (used for production test and acceptance procedures during the first six months of production shipments)

b. Remote or local terminal via modem

E.7.2.1 Off Line – The OFF LINE test/diagnostic procedures exercise 100 percent of the modem control hardware up to the point of demarcation at the modem interface. The OFF LINE test requires two configurations (Figures E-4 and E-5) to achieve 100 percent testing.

Hardware requirements are as follows:

1 PDP-11 with > 4K core
1 DH11-AD System Unit (modules not required)
1 Modem Control Module Set (M7807 and M7808)
1 H861 Test Connector (16 lines)
1 H315 Modem Test Connector (1 line)
4 BC08R Cables
1 BC05D-25 modem cable
1 MAINDEC-11-DZDHK

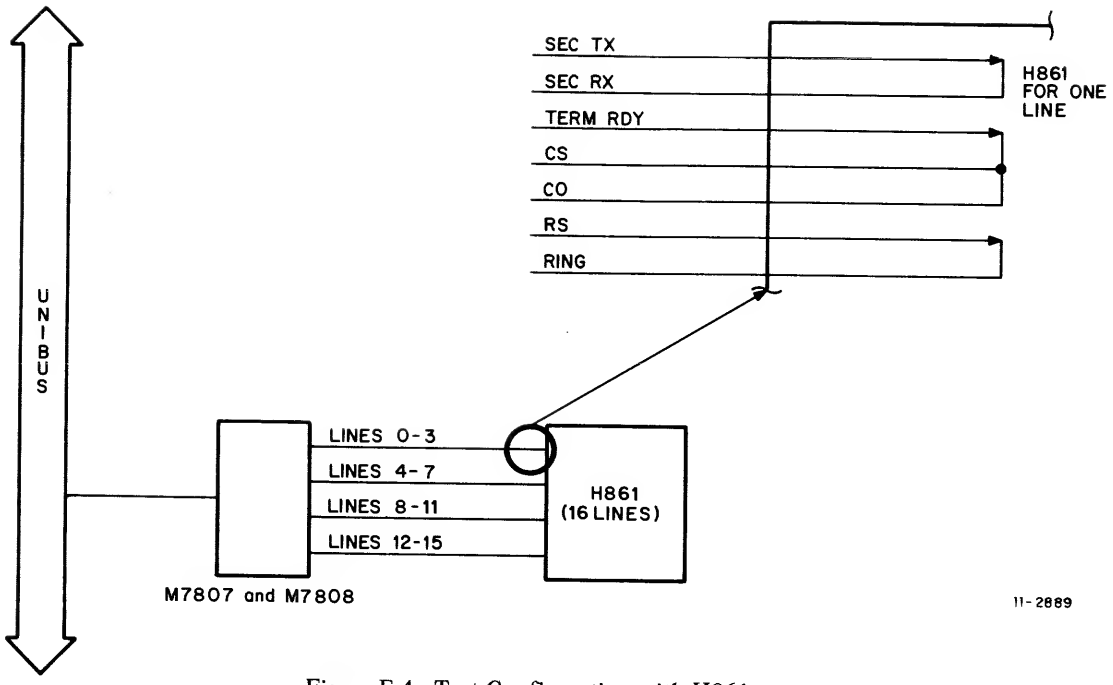


Figure E-4 Test Configuration with H861

OFF LINE – Terminated with H861

Step	Procedure
1	Assemble hardware per Figure E-4.
2	Operate MAINDEC-11-DZDHK per MAINDEC procedures.
3	Five or more passes is considered a valid test.
4	Assemble hardware per Figure E-5.
5	Operate MAINDEC-11-DZDHK per MAINDEC procedures.
6	Five or more passes is considered a valid test.

E.7.2.2 On Line – The ON LINE Test/Diagnostic will function with limited configurations and is intended to perform a confidence test, in that the control will adapt to 103, 202, and 811B (or equivalent) type modems. The 811B configuration is left out as the 202 satisfactorily exercises all of the active elements used with the 811B Interface.

The ON LINE test utilizes two configurations as illustrated in Figures E-6 and E-7. Figure E-6 utilizes two modems: they may be either two 103As or two 202Cs.

Figure E-7 provides an ON LINE test for up to 16 lines to a local or remote terminal. In this configuration, the modem control is operated in the Auto-Answer mode. The modems connected are 103As, while those connected to the terminal may be 103As or acoustic couplers.

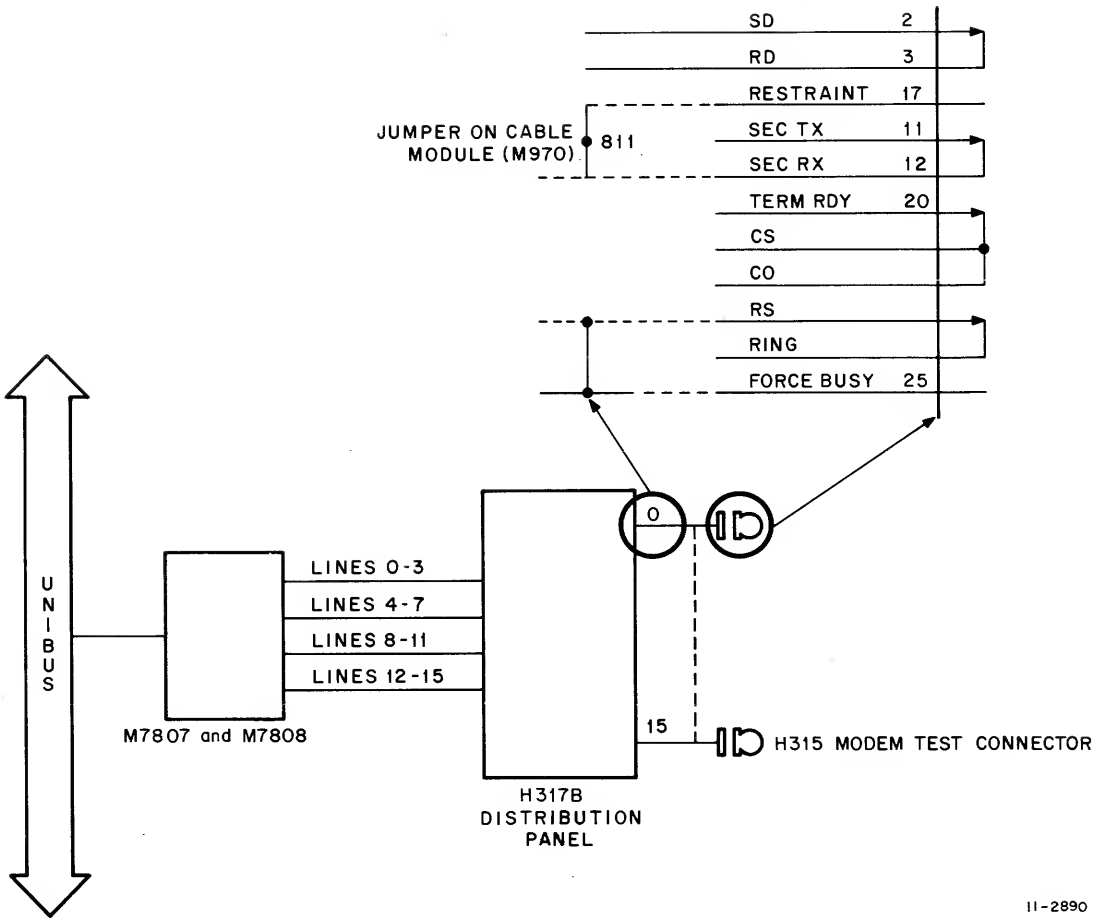


Figure E-5 Test Configuration, Distribution Panel and Test Connector

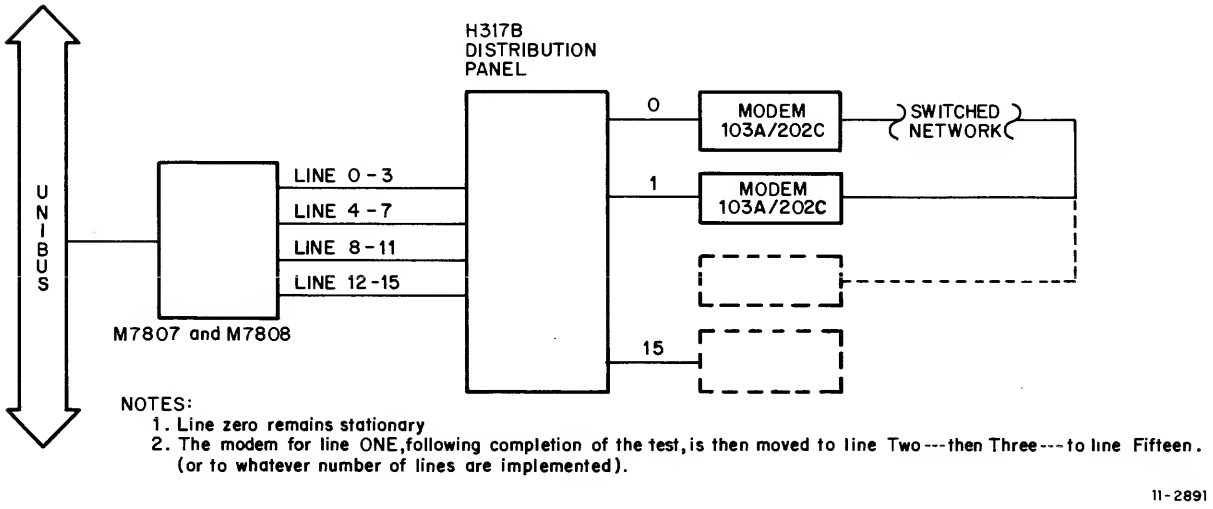


Figure E-6 Test Configuration (ON LINE Modem Loop Back)

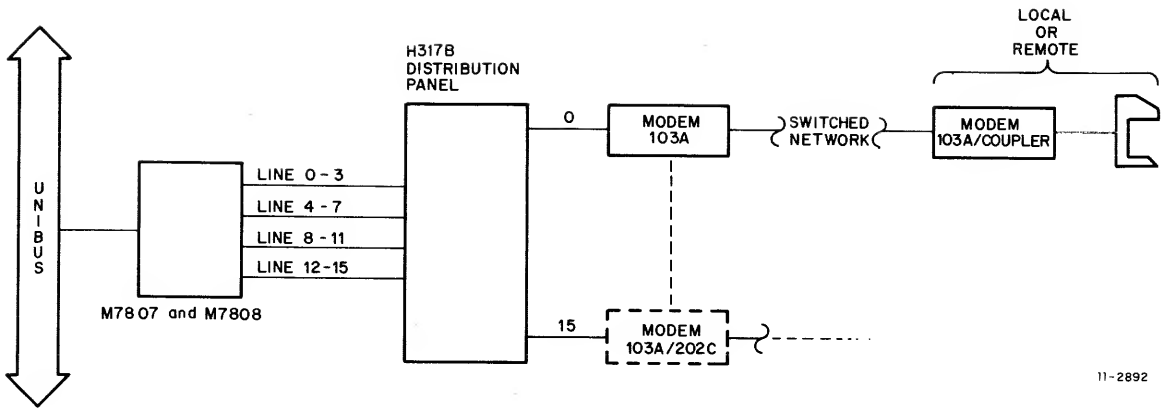


Figure E-7 Test Configuration (ON LINE Modem to Terminal)

The hardware required is:

1 PDP-11 with > 4K Core
1 DH11-AD
1 modem control module set (M7807 and M7808)
4 BC08R Cables
A/R Modems (103A or 202C)

ON LINE – Modem Loop

Step	Procedure
1	Assemble hardware per Figure E-6.
2	Connect a modem (originate) to Line 0.
3	A second modem (answer) should be connected to any line that requires a test (Lines 1 through 15).
4	Operate MAINDEC-11-DZDHK per MAINDEC procedures.
5	Five or more passes is considered a valid test.

ON LINE – Modem to Terminal

Step	Procedure
1	Assemble hardware per Figure E-7.
2	Connect modem (103A) as required to lines 0 through 15. These modems should be connected for Auto-Answer mode of operation.

NOTE
The terminal should originate all communications channels.

Step	Procedure
3	Operate MAINDEC-11-DZDHK per MAINDEC procedures.
4	Satisfactory transfers to (from) the terminal(s) is considered a valid test.

APPENDIX F
MODEM TIMING AND FLOW DIAGRAMS

This appendix provides the timing and flow diagrams for some modems utilized with the modem control. Diagrams are for reference information and are as follows:

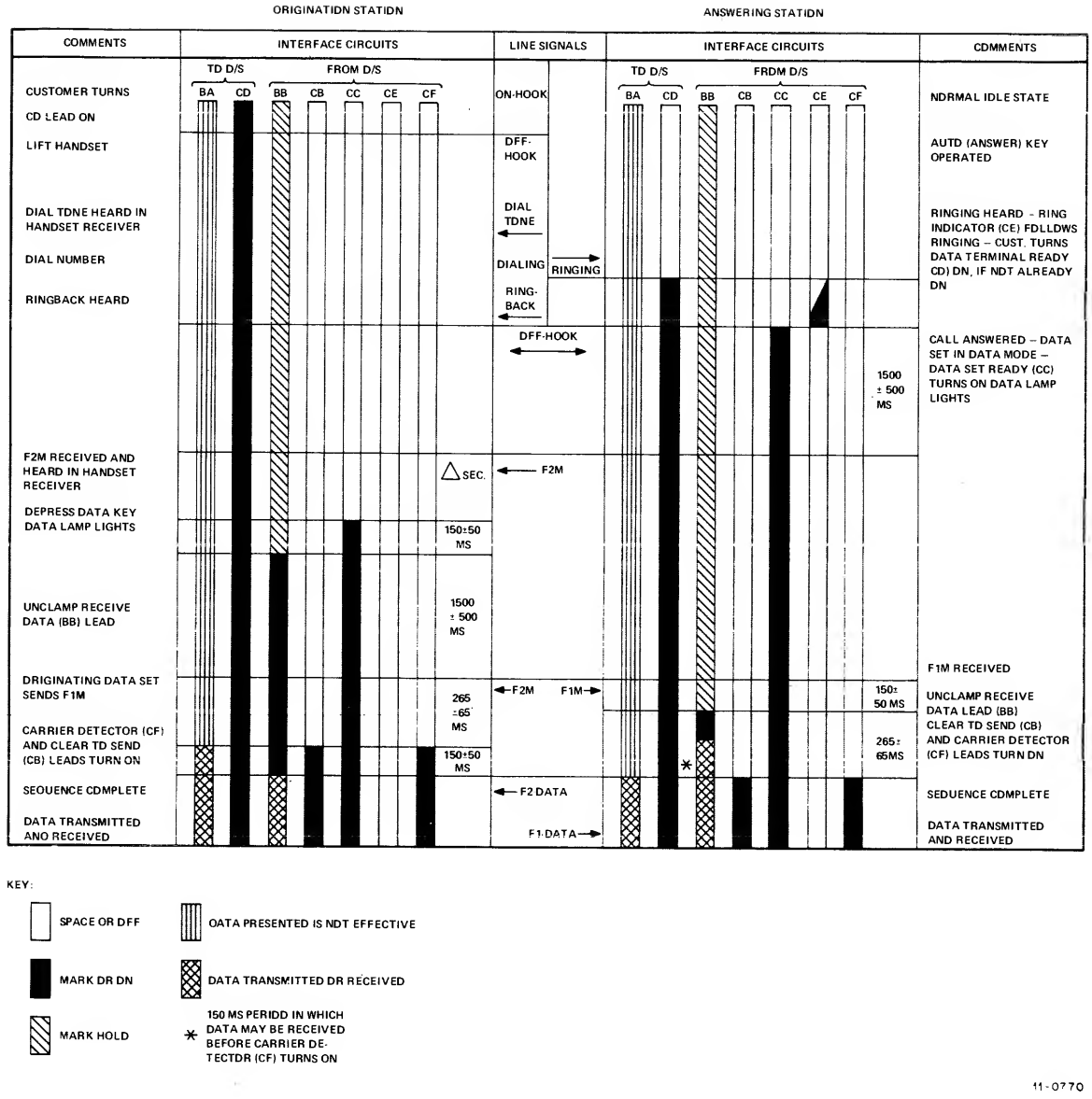


Figure F-1 Data Set 103A Channel Establishment Sequence

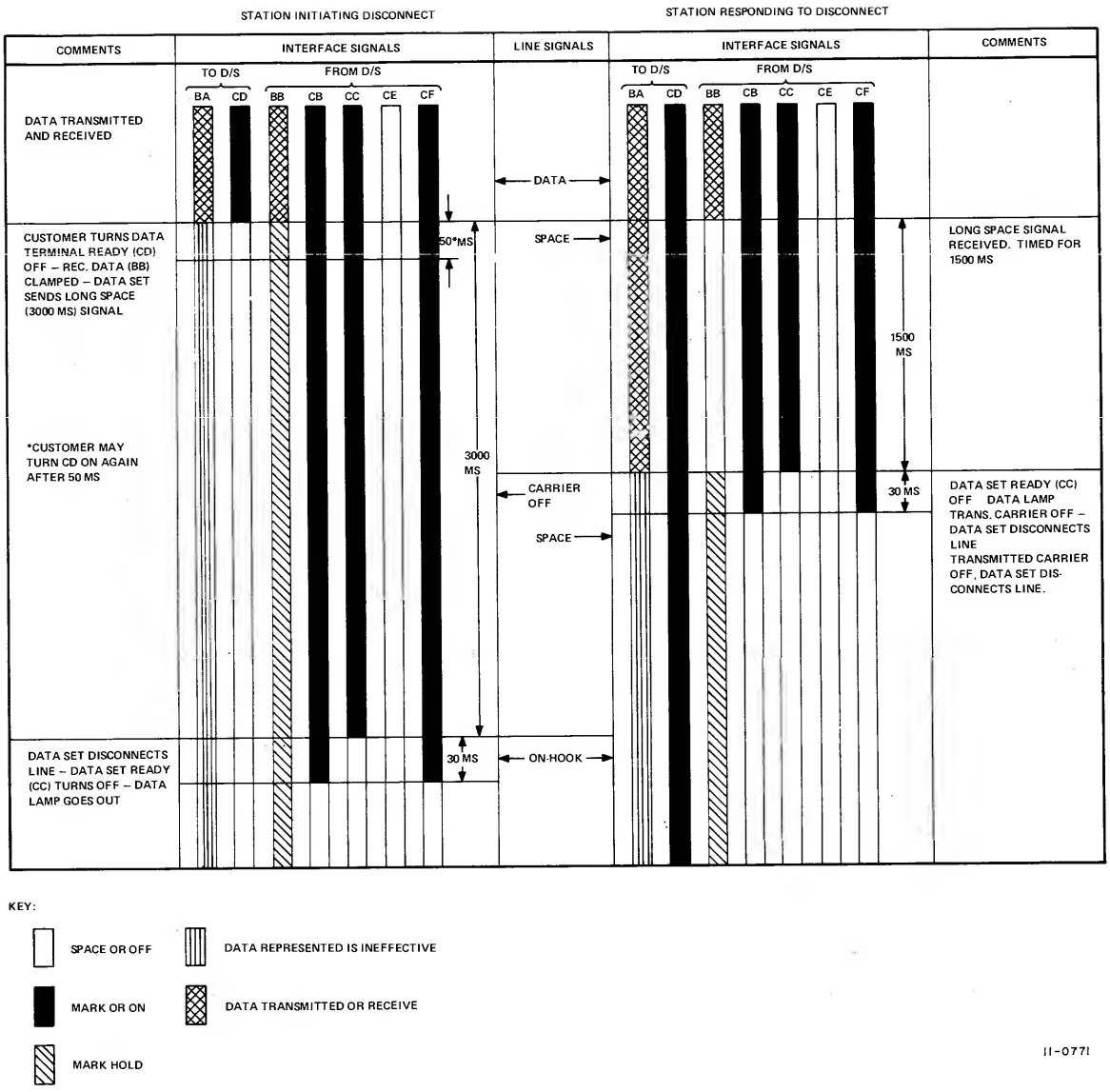


Figure F-2 Data Set 103A Space Disconnect Sequence

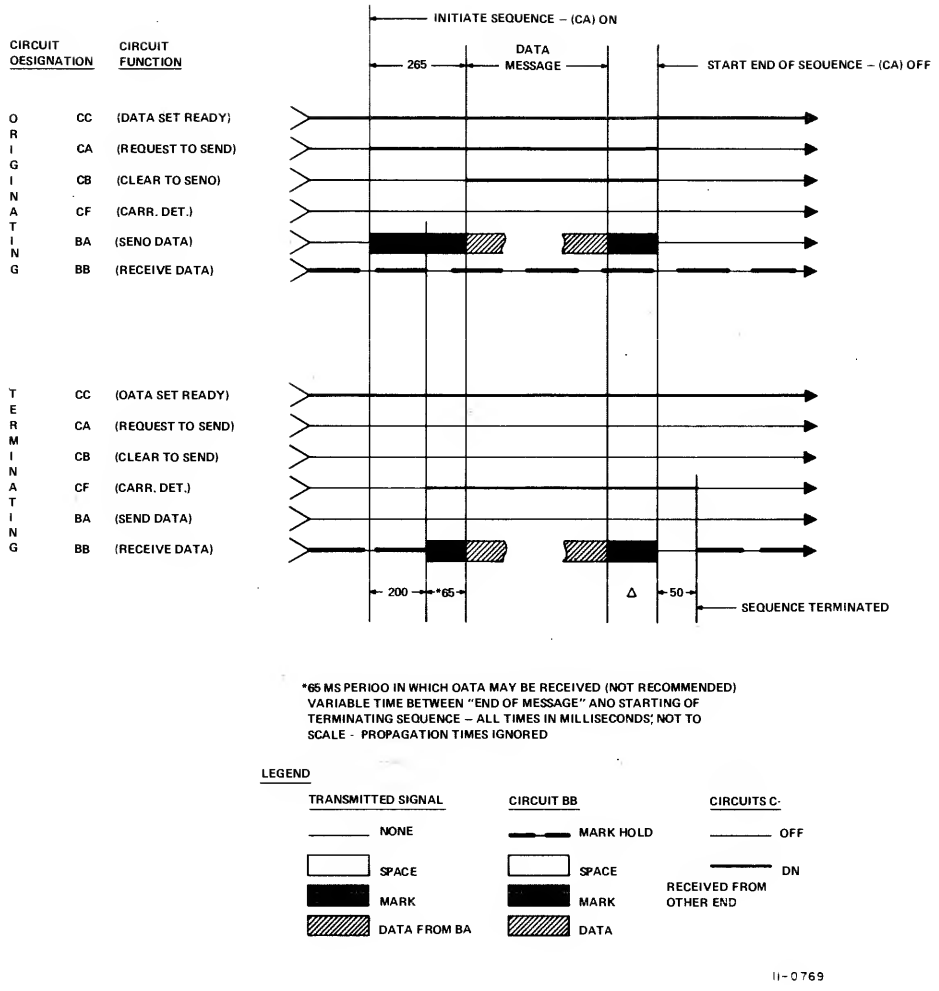


Figure F-3 Data Set 103F Timing Sequence

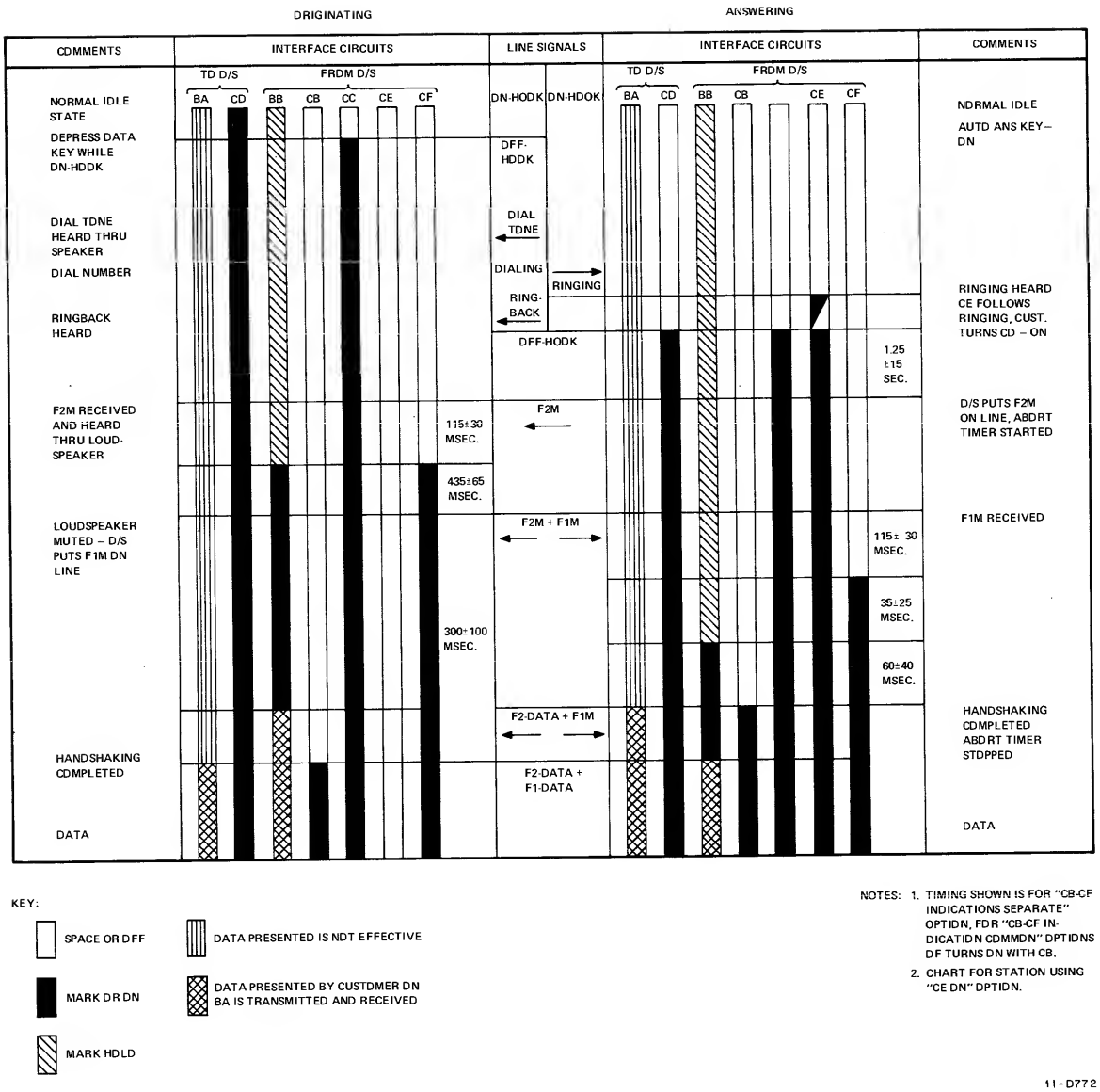
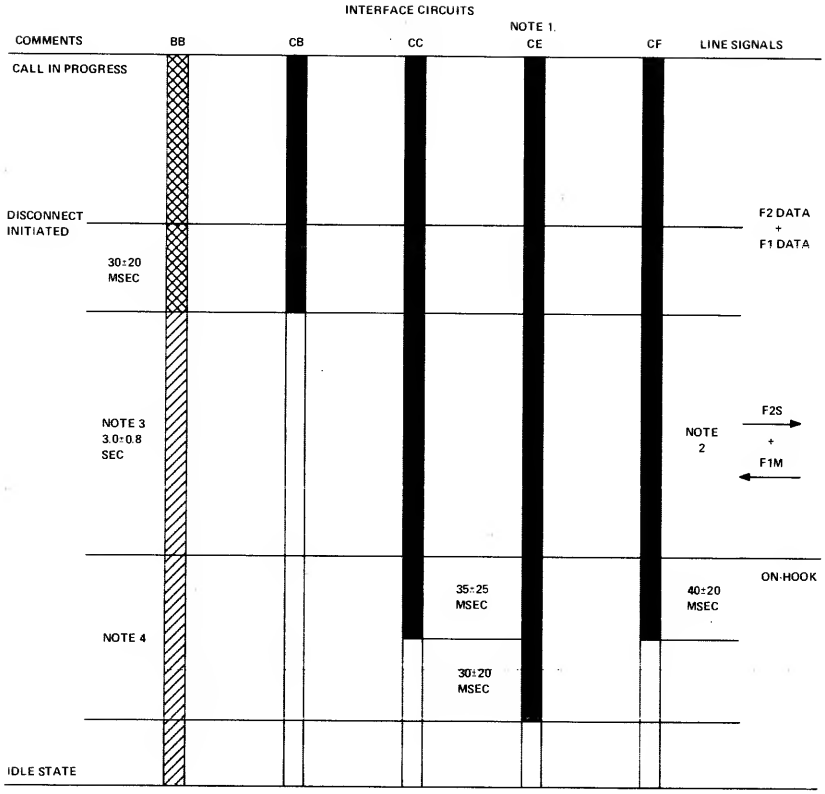


Figure F-4 Data Set 103E Type Sequence Chart for a Call Originated in the Semiautomatic Manner and Answered Automatically

DISCONNECT INITIATED BY EITHER
A) BUSINESS MACHINE TURNING CKT. CD OFF
B) ATTENDANT DEPRESSING CLEAR KEY, OR
C) AUTOMATIC CALLING UNIT SIGNALING DATA SET TO DISCONNECT



NOTES
1. FOR ANS MODE STATION WITH "CE-ON" OPTION.
2. IF THE OTHER STATION IS WIRED TO DISCONNECT ON SPACE, CF WILL GO OFF DURING THIS INTERVAL.
3. TIME SHOWN IS FOR "SEND DISCONNECT-YES" OPTION. TIME FOR "SENO DISCONNECT-NO" DPTION IS 30±20 MSEC, IF DISCONNECT IS INITIATED BY CD OFF. OTHERWISE TIME IS AS SHOWN.
4. SEQUENCING OF TURN-OFFS MAY BE EITHER CF, CC, CE, OR CC, CR, CE, OR CC, CE, CF.
5. TIME SHOWN IS FOR "CB-CF INDICATIONS SEPARATE" OPTION. FOR "CB-CF INDICATIONS COMMON" OPTION, CF TURNS OFF WITH CB.

11-0773

Figure F-5 Data Set 103E Type Detailed Disconnect Sequences

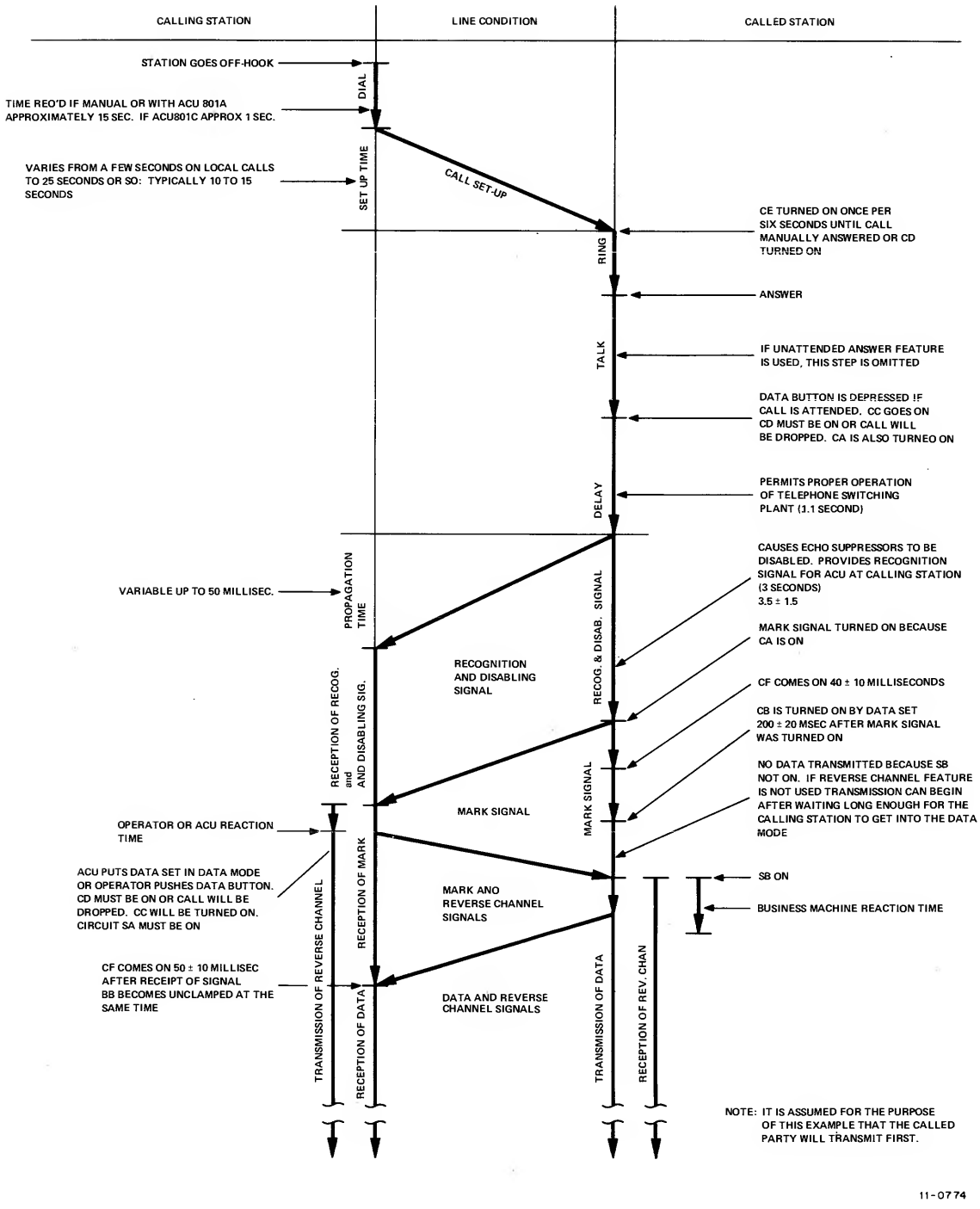


Figure F-6 Establishment of a 202C Call

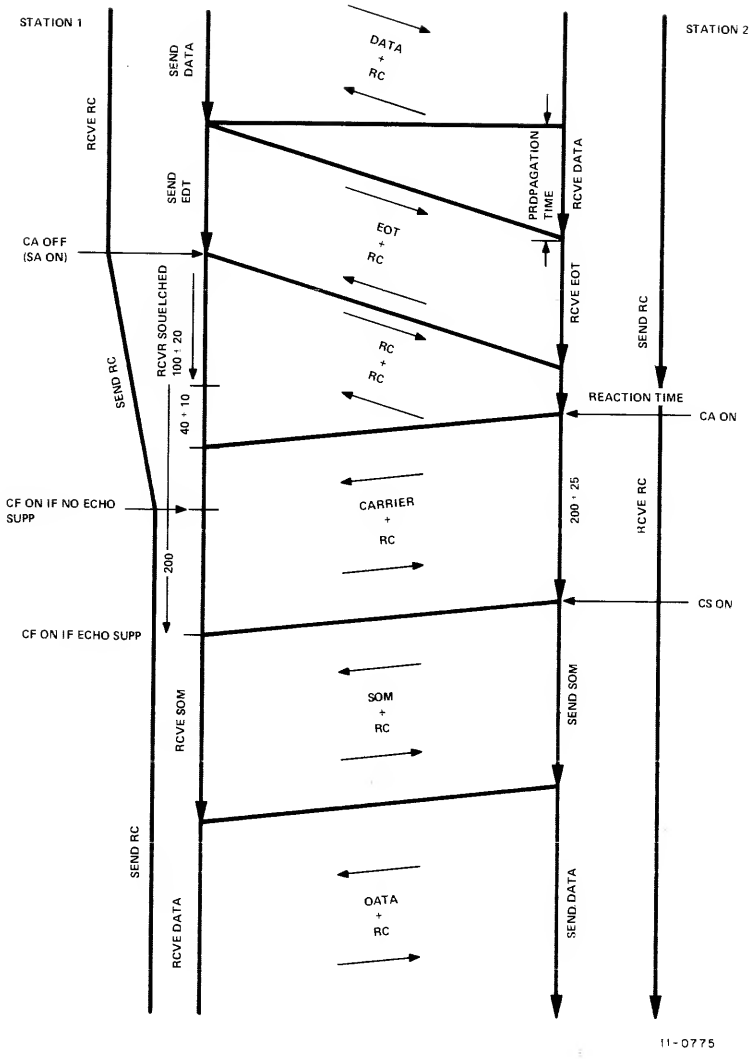


Figure F-7 Turn Around In Data-Phone Service 202C

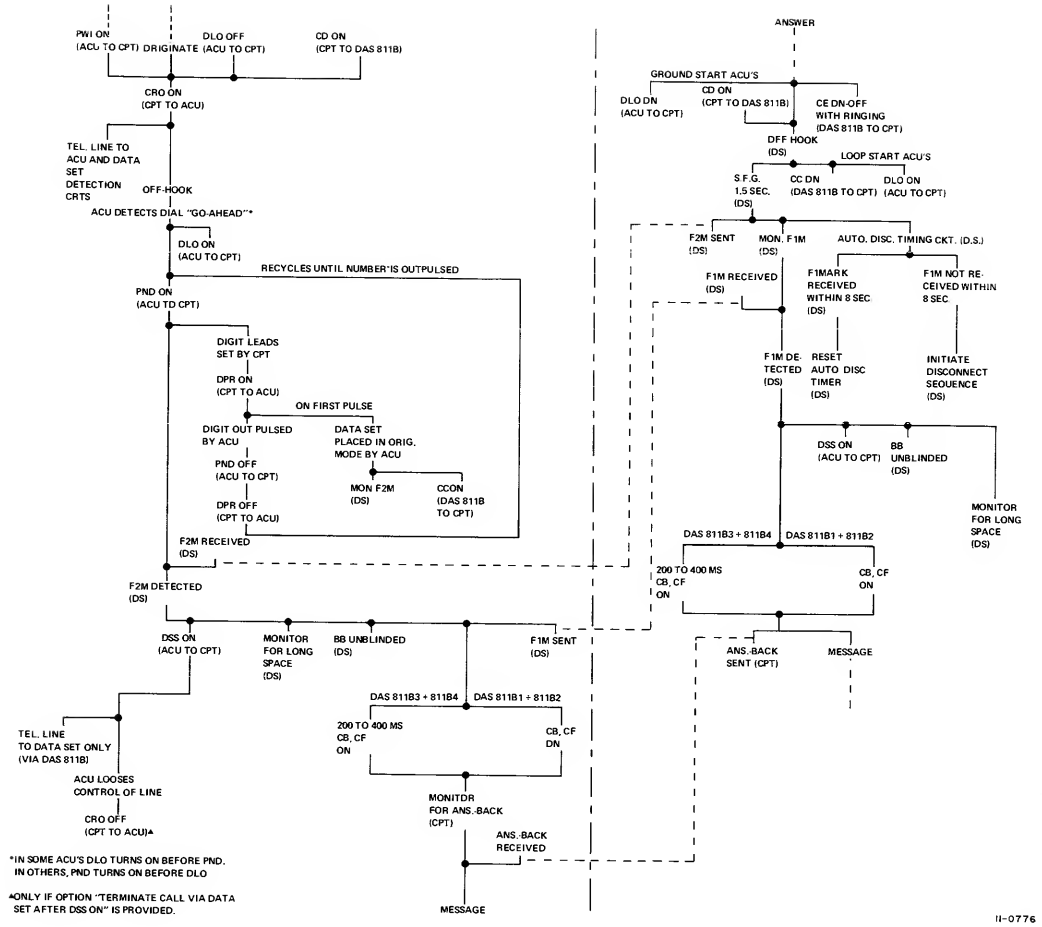


Figure F-8 811B Originating and Answering Flow Chart
for CPT for 3 or 4 Row TWX Service Data Set Tone Detection without EON

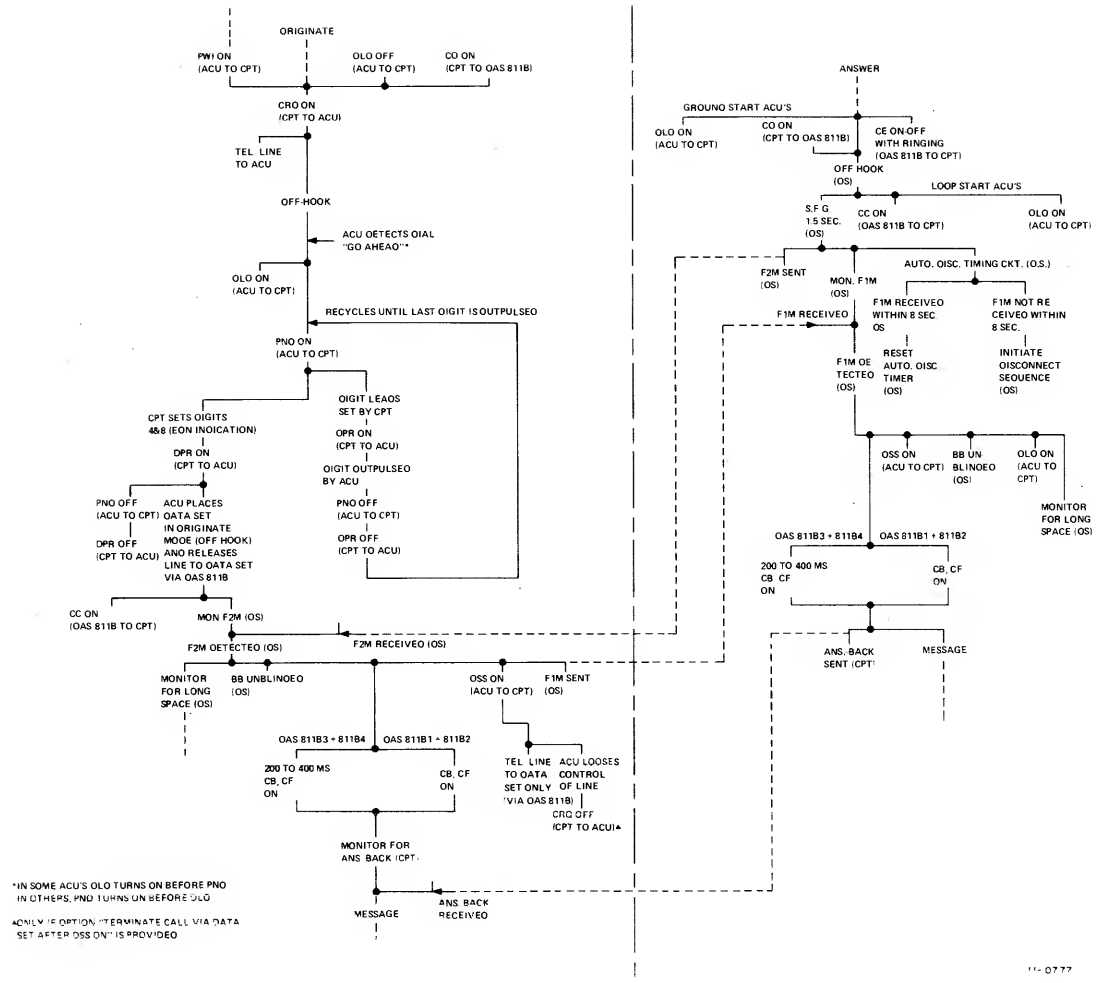


Figure F-9 811B Originating and Answering Flow Chart
for CPT for 3 or 4 Row TWX Service Data Set Tone Detection with EON

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